

AMSTRAD CPC CRT COMPENDIUM V1.2



LOGON SYSTEM

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1 PREFACE

The objective of this document is to provide detailed information on the operation of the various CRTC 6845 circuits implemented in the CPC's created by AMSTRAD. The CRTC is a controller circuit capable of providing an interface between microcomputers and cathode ray screens that manage video scanning.

The document also discusses the operation of some circuits associated with the CRTC's, especially the GATE ARRAY.

Game or demo programmers still working on these machines designed in the 1980s and the 1990s may find the information presented here useful.

It can also serve as a reference for anyone wishing to create an emulator by adapting code ad hoc for specific programs.

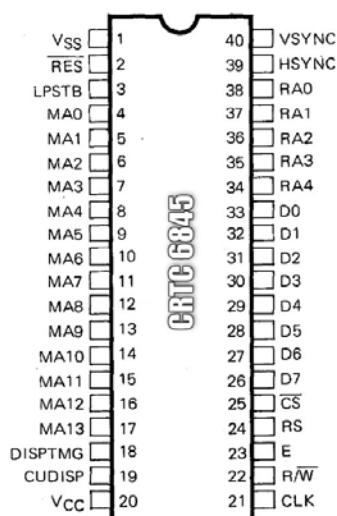
Finally, this document may provide useful information to users of other machines equipped with similar CRTC's. However, it must be noted that the timing between the processor, the CRTC and the associated video circuit of another machine can significantly modify the behaviours described here. Furthermore, the document only describes the CRTC functions used on the CPC; "text" mode and the "cursor" are therefore not discussed here.

Part of the information presented in this document has been checked using a benchmarking program called SHAKER. It was tested for each CRTC on several machines, and the photos obtained from the results of each test have been compiled into separate documents, one per CRTC.

Truth takes up little space, but error occupies an infinite number of places.
This document is subject to revision and change.

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2 VERSION HISTORY

Version	Date	Update
1.0	01/01/2021	Document created. Proofreading: Arnaud Storq, Claire Dupas, Sébastien Broudin
1.1	15/12/2021	Diagrams reimported. Corrections made in §4.3, 4.5, 7.2. Statuses grouped together in § 21 with addition of read registers and definition of CRTC 3 & 4 statuses. CPI/CPD/CPIR/CPDR instruction duration corrected.
1.2	01/01/2022	Major update. Precisions, corrections and clarifications on some chapters (especially on CRTC 0: VSync, C9 freeze on R0=0, Interlace Modes). New chapters on the GATE ARRAY (horizontal splitting mode, hsync, interrupts). Description of the RFD. Vertical scroll at 1/64th of a pixel. Proofreading: David Manuel, Claire Dupas, Olivier Antoine

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3 GENERAL

3.1 TERMINOLOGY

The CRTC is a circuit that spends its time counting and comparing.

It therefore mainly consists of counters, the limit value of which is generally defined in the programmable registers of the circuit.

With the goal of constructing screens made of several vertical characters, in turn made of several vertical lines, which in turn is made of several horizontal characters, certain terms are associated with these registers and counters.

We therefore speak of "*horizontal total number of characters*", "*vertical total number of characters*" and "*Maximum Raster*" to define the value of certain registers, with some differences on occasion depending on the technical documentation under consideration. Some emulators use "unofficial" acronyms to define the names of associated counters: HCC, VTAC, VLC, VCC, ... to name a few.

These terms are no longer appropriate when working at a level other than that intended for the construction of a "standard" screen.

Indeed, at a certain level, the logic of "horizontal" and "vertical" counting practically disappears. It then becomes difficult to speak of "characters" without tripping on one's shoelaces, as depending on the circuit's programming, a vertical character can also be a horizontal character.

This notion exists at most in relation to the synchronization logic of the constructed screen.

Since it is possible to reduce the size of a line to 1 μ sec, to reduce the size of a vertical character to 1 line and to reduce the size of a screen to 1 character, the horizontal and vertical qualifiers somewhat lose their meaning.

For these reasons, I will generally denote the CRTC registers in this document as **Rn** and the associated counters as **Cn**. "Characters" will denote the words processed by the GATE ARRAY from the address provided by the CRTC. I have named the CRTC's two internal pointers VMA and VMA'.

I invite the authors of emulators based on this document to adopt these notations. Here are equivalents for some of the terms that I have encountered:

Names identified in certain emulators	Counters
HCC (Horizontal Char Counter)	C0
VLC (Vertical Line Counter)	C9
VCC (Vertical Character Counter)	C4
VSC (Vertical Sync Counter)	C3h
HSC (Horizontal Sync Counter)	C3l
VTAC (Vertical Total Adjust Counter)	C5 or C9 (on CRTC 0)
VMA (byte pointer)	VMA or VMA' (word pointer)

3.2 ACRONYMS

ASIC : Application Specific Integrated Circuit : Integrated circuit which groups on the same chip all the functions necessary for a specific application. The GATE ARRAY is an ASIC.

CRTC : Cathode Ray Tube Controller: Circuit used to interface a computer with a cathode ray monitor capable of handling raster lines.

HBL : Horizontal BLank Line: Refers to the period during which the monitor's electron beam, which has reached the right side of the monitor, turns off the beam to return to the left of the screen.

HSYNC : Horizontal SYNC: Refers to the signal emitted by the CRTC which allows the monitor (via the GATE ARRAY on CPC) to synchronize the screen horizontally.

IVM : Interlace Video Mode.

IS : Interlace Sync.

PIXEL-M2 : Definition of a pixel displayed in graphics mode 2 (0.0625 μ sec).

RFD : Rupture for Dummies on CRTC 1.

RLAL : Rupture Ligne à Ligne (from French). Definition of a rupture where the video address can be updated on each each raster line of the screen.

RV : Rupture Verticale (from French): Definition of a rupture whose axis is not "horizontal", and where horizontal zones can be created.

RVI : Rupture Verticale Invisible (from French) : Refers to vertical ruptures occurring during the Hsync and not visible.

RVLL : Rupture Verticale Last Line (from Frenglish): Refers to vertical ruptures using the C4 « last line » processing on CRTC's 0 and 2.

VBL : Vertical BLank Line : Refers to the period during which the monitor electron beam, which has reached the bottom of the screen, deactivates the beam to return to the top of the screen.

VMA : Video Memory Address : CRTC pointer to the words addressed in memory and supplied to the GATE ARRAY for display.

VSYNC : Vertical SYNC : Signal emitted by the CRTC which allows the monitor (via the GATE ARRAY on CPC) to synchronize the screen vertically.

4 CRTC & CPC...

4.1 GENERAL

On the AMSTRAD CPC, the duration of a CRTC character is 1 μ sec..

This CRTC character represents 2 bytes in memory.

The memory pointer is **communicated by the CRTC to the GATE ARRAY, which will always read the "central ram" of 64k**. The GATE ARRAY cannot read the data in ROM or in the additional RAM of 6128s (or memory extensions) except for TotOs intervention.

The CRTC is programmed so that the image thus created is supported by a monitor. A language shortcut is to use the term NOP instead of μ sec (microsecond) because it is the time taken by this instruction in Z80A on CPC.

On CPC, the Z80A instructions are aligned by rounding the M cycles of an instruction to a multiple of 4 T cycles. This alignment is linked to the need for the GATE ARRAY to interrupt the Z80A to access the ram whose address is provided by the CRTC. This operation slows down some instructions relative to the clock frequency. Achieving accurate code requires knowing the exact time taken by each instruction. See Chapter 24, page 214, for details of these durations for each instruction.

A bit of history

Old Cathode ray monitors and televisions lined up their display frequency with the electricity distribution network of the country of marketing.

In Europe in particular, televisions built to support SECAM and PAL formats operate with a horizontal frequency of 15625 Hz, and a vertical frequency of 50 Hz.

Note that the American (and Japanese) format was the NTSC (National Television System Committee) with a horizontal frequency of 15734 Hz and vertical of 60 Hz.

The horizontal frequency of 15625 Hz comes from the use of 64 μ s delay line, invented for the design of the Secam format by the engineer Henri de France. As a reminder, 64 μ s = 0.000064 seconds (just enough time to have a strong coffee).

The CRTC follows this logic and processes about 1 million characters per second because its frequency is 1 MHz.

Without diabolical intervention on the position of the HSYNC, it is in principle programmed to generate complete lines of 64 μ sec.

To get closer to the desired frequency, the CRTC is generally programmed to display 312 lines of 64 μ s, or exactly 19968 μ sec (0.019968 seconds).

This frequency being linked to a clock, we can see drifts between 2 machines after a certain time.

The standard format initialized by the CPC ROM in a European country is :

- Lines of 64 horizontal "CRTC" characters of 1 μ s each (composed of 40 characters displayed and 24 not displayed).
- 312 vertical lines, subdivided into vertical characters of 8 lines, or 39 characters.
- Formula : $((R4+1) \times (R9+1)) + R5$
- Of these 39 character lines, 25 are displayed.
- CRTC table ROM address: **&5C5**

The standard format initialized by the CPC ROM in the United States is:

- Lines of 64 horizontal "CRTC" characters of 1 μ s each (composed of 40 characters displayed and 24 not displayed).
- 262 vertical lines, sub divided into vertical characters of 8 lines, or 32 characters + 6 lines of adjustment
- Formula : $((R4+1) \times (R9+1)) + R5$
- Of these 32.75 character lines, 25 are displayed.
- CRTC table ROM address: **&5D5**

Note 1 : It is the bit 4 of port B of the PPI (LK4) that allows you to test which table to use.

Note 2 : Initializing the CRTC is one of the first things the CPC's LOW ROM does when the machine is turned on and reset. Register initialization begins 64 μ sec after the Z80A reads the first ROM instruction. Registers are updated from register 15 to register 0.

CTM monitors use the PC1031 (GT65 green monochrome monitor) and PC1378 (CTM 644 colour monitor) circuits. These circuits are used to drive the horizontal deflector to produce the signal the beam needs for scanning.

The GATE ARRAY of the CPC produces, via its pin 5, a composite synchronization signal combining VSYNC and HSYNC, which arrives at the DIN connector provided for the monitor (via a 220 Ohm resistor (R137)).

This composite signal is decoded by the circuits (PC1031 or PC1378) of the monitor. [Since the monitor is not a TV, the signals for the image are always RGB]

The CRTC has registers to manage a cursor and read data sent by an "optical pen". Cursor registers are not used on CPC, which does not handle a hardware cursor, usually provided when a text mode is handled.

However, they are a point of interest, because actions on other registers in or out of a synchronization period, with small values, could lead to consequences on other registers.

The operation of these registers is not covered (at the moment) in this document.

4.2 CRTC TYPES

AMSTRAD had the brilliant idea of using CRTC 6845 circuits manufactured by different manufacturers in its machines. They even designed ASIC's that could emulate its operation.

A bit of history

While Amstrad wanted to attack the US market with the CPC 6128, a problem was identified in ROM with registry value 5 (vertical adjustment).

This value was set at 6 in accordance with the desired frequency of 60Hz in the USA (262 lines), but (wrongly) ignored the interrupt system managed by the GATE ARRAY. Indeed, on a European CPC, interruptions start 2 lines (we will consider that we have 1 HSYNC per line) after the occurrence of the VSYNC signal by the CRTC.

These interruptions have a period of 52 "HSYNC lines", which gives exactly 6 periods during the 312 lines (see Chapter 25.6 on INTERRUPTS). To stall 5 periods of 52 lines, it would have been necessary to program 260 lines and not 262 as was done, and therefore that R5 is programmed with 4 instead of 6.

These 2 more lines cause the interruption to arrive on not the same line on which the CRTC reports the start of VSYNC, BUT before it.

That is, on a US CPC, a program whose main code tests the VSYNC wait via the PPI can be interrupted during this wait. If the interruption lasts too long, when it returns, the VSYNC waiting loop has missed the signal (the bit has returned to 0), and a risk of "deadlock" exists.

This could lead to compatibility issues for programs produced in Europe. AMSTRAD then decided to remedy the problem bychanging the 60 Hz table to ROM....

No... I'm kidding... too simple.

To avoid this "deadlock" without modifying the ROM, Amstrad engineers thought they could "limit the problem" by increasing the duration of the VSYNC. This was perfectly possible using the CRTC's Registry 3, which had been programmed with 8 lines in the ROM.

It is likely that they thought that there were CRTC models without the function used to set the number of VSYNC lines (these models set the number of lines at 16) and thus decided that the American CPCs would only be equipped with CRTC's 1 and 2, without this function.

If AMSTRAD engineers were aware of the existence of these differences, it can be assumed that the first CRTC's used were type 0s, since this function is used and programmed by the ROM.

From there to be able to say that without a bug related to a 4 instead of a 6 in the ROM, there would be only one type of CRTC used in all CPC's, it is to ignore the commercial considerations in the component market compared to the success of the machine in Europe.

Several companies have created different versions of the circuit, implementing additional functions, such as programming the number of lines of the VSYNC that I have just mentioned.

It can be deduced, however, that the designers of the BASIC ROM:

- originally worked with a CRTC with the ability to program the number of lines for VSYNC.
- felt that 8 lines of VSYNC were sufficient to vertically synchronize the image on a CTM monitor.

Beyond the functional and technical differences documented in circuit manufacturers' guides (called "datasheets" with 2 "e"'s), these CRTC's tend to behave differently when starting to modify registers:

- multiple times during a frame.
- during or outside HSYNC/VSYNC periods.
- with a value of 0, which is a special case for managing multiple registers.

These differences impact the compatibility of programs, especially when the address of the video pointer is updated.

This technique is still commonly called "*Rupture*" because... it is simpler and more generic than to say "*Offset Split Screen*".

Differences in counter management (which can overflow in a few situations) usually lead to a horizontal (R2) and/or vertical (R7) synchronization defect.

If a Z80A code "waits" for the VSYNC signal or uses interrupts (which depend on HSYNC), the mess is accentuated.

A bit of history

To my knowledge, the first program to have carried out a CRTC test was the game "Get Dexter" ("Crafton & Xunk" in French), written by Rémi Herbulot and Michel RHO in 1986. In this game, the screen update takes place through horizontal scrolling, which uses register 2 (positioning the HSYNC on another character).

This method, on a MOTOROLA CRTC, causes a loss of vertical synchronisation when VSYNC occurs during a HSYNC (Ghost Vsync). In other words, in this situation, the CRTC falsely believes it is generating a VSYNC signal for the monitor.

I guess Rémi Herbulot had to have access, at Ere Informatique game company, to a CPC with a HITACHI CRTC (like mine at the time) and another with a MOTOROLA CRTC. Having made this observation, he created a test based on the reading in &BFO0 of register 12, which makes it possible to distinguish the CRTC HITACHI from the CRTC MOTOROLA.

And so, he managed a display with and without scrolling on the screen.

That is why there is no scrolling in this game on CPC's equipped with a UMC CRTC, while this CRTC does allow it without issue, because as with the MOTOROLA CRTC, its register 12 is not readable.

A bit of history (yet !)

When the first "rupture" techniques began to be used massively in demos, the differences between CRTC soon began to be a problem. And especially when independent programmers (often high school or university students) began to form the "demo" scene and their demos began to circulate in a less discretionary way. Initially, these first demos were mostly introductions for cracked games that circulated in schoolyards. [I believe there is a game from the 80s that encountered this type of problem with the CRTC (to be checked)]

The first demo programmers had not yet built up a "network" (the demoscene) and usually had only one machine on hand. The first intros and demos circulated in a small and very regional circle. The "network" consisted, in the 80s, of postal exchanges, Minitel's (a French ancestor of the internet, like Prestel in the UK) and ruinous telephone exchanges, with very little or no relations with other countries.

Communication with people from other regions first went through the consultation of classified ads in the few computer magazines of the time, because it was difficult to find contact details in the introduction preceding a cracked game. Programmers could hardly see the result produced by their code on other machines, and the inertia was enormous. It was difficult to adapt the code via postal exchanges, without having the machine (or even wanting to do it, simply). The problems encountered could range from image synchronization-loss to outright crashing of the machine.

It was difficult to be categorical about the actual origin of these problems, and especially about their extent. Nevertheless, with the grouping of the demomakers and the enlargement of the demoscene, it became possible to compare the code on different machines.

The presence of some electronics engineers in the ranks of the demomakers made it possible to identify the culprits... (Mr. SUGAR is still at large).

Some "universal" rules resulting from empirical approaches have been described in secret documentation which did not remain so for long ("You should not do this operation here in order for it to work everywhere", for example).

It should be noted that some techniques are still currently considered impossible to port from one CRTC to another (until this document...).

CRTC 2 (MOTOROLA) quickly proved to be the problematic one for one of the most widely used techniques, which is to place $R4=R9=0$.

The code needed to ensure CRTC compatibility can be much more complex than just knowing when to modify register 9 or 4, we'll see...

In order to exploit the rules allowing compatibility, it was first necessary to identify the different CRTC's.

Many methods exist today. See Chapters 26, page 223, and 27, page 225.

The numbering has remained fixed to this day from the order where I discovered these circuits with the help of some members of the group of demomakers Logon System.

We discovered the CRTC emulated "Pre ASIC" after the release of the AMSTRAD PLUS, and that's why its number is greater than 3, although it came out earlier chronologically.

Type	Brand	Model
0	HITACHI	HD6845S(P)
0	U.M.C. (United Microcircuits Corporation)	UM6845
1-A	U.M.C. (United Microcircuits Corporation)	UM6845R
1-B	U.M.C. (United Microcircuits Corporation)	UM6845R
2	MOTOROLA	MC6845(P)
3	AMSTRAD	ASIC 40489
4	AMSTRAD	ASIC 40226

Note 1 : CRTC's 3 and 4 are CRTC's emulated by ASIC's, but are nevertheless CRTC! Without enabling the complementary functions of ASIC 40489, the behaviour of these two CRTC's cannot be differentiated at present.

Note 2 : The "Pre-ASIC" (CRTC 4) was most certainly designed with the AMSTRAD PLUS in mind, as its C9 counter is intended to be interrupted on any line. This is why positioning R9 at 0 can be done on the last line of a character (CRTC 0 compatibility) or on the first line of a character (CRTC 1 compatibility).

Note 3 : It cannot be excluded even at present, that some series of CPC's may be equipped with different CRTC models, available from the 3 manufacturers. (Please let me know if you discover another model, and you are sure that it was not your little sister who replaced it for a laugh). Additionally, HITACHI's CRTC HD6845S, which is identified as type 0, behaves exactly like UMC's CRTC UM6845. Probably a business deal between the firms where it is just the manufacturer marking that has changed... The UMC documentation specifies this in its comparison table with other circuits. There is currently no test that allows the distinction of these two circuits, but it may be possible via the "Interlace" mode or the special management of C0 by the HD6845S.

Note 4 : Programming R3 with &8x is a very bad habit, since CRTC's 1 and 2 also exist in European machines, and they do not respect this value...

Note 5 : Scheduling a specific update to a CRTC register in an interrupt routine that does not interrupt perfectly synchronized code is a very bad idea. (And may suggest (wrongly) a CRTC difference).

Note 6 : The difference observed between two CRTC's UM6845R may not be linked to the CRTC. Nevertheless, there is a noticeable difference. (See Chapter 11.5)

4.3 GENERAL VIEW OF THE REGISTERS

Register	Definition	Unit	CRTC 0								CRTC 1, 2								CRTC 3, 4										
			r/w	7	6	5	4	3	2	1	0	r/w	7	6	5	4	3	2	1	0	r/w	7	6	5	4	3	2	1	0
R0	Horizontal total character number	Char	w								w									w									
R1	Horizontal displayed character number	Char	w								w									w									
R2	Position of horizontal sync. pulse	Char	w								w									w									
R3	Pulse width of horizontal sync. pulse	Function	w	v	v	v	v	h	h	h	w					h	h	h	h	w	v	v	v	v	h	h	h	h	
R4	Vertical total character number	Char Row	w								w									w									
R5	Total raster adjust	Scan Line	w								w									w									
R6	Vertical displayed character number	Char Row	w								w									w									
R7	Position of vertical sync. pulse	Char Row	w								w									w									
R8	Interlace Mode and Skew	Function	w	c	c	d	d			i	i	w						i	i	w	c	c	d	d			i	i	
R9	Max Scan Line Address	Scan Line	w									w								w									
R10	Cursor start	Scan Line	w		b	p						w		b	p					r	s	1	s	s	s	s	s	s	
R11	Cursor end	Scan Line	w									w								r	s	0	s	1	s	s	s	s	
R12	Display start address (High)	Pointer	r/w									w								r/w									
R13	Display start address (Low)	Pointer	r/w									w								r/w									
R14	Cursor address (High)	Pointer	r/w									r/w								r/w									
R15	Cursor address (Low)	Pointer	r/w									r/w								r/w									
R16	Light Pen (High)	Pointer	r									r								r									
R17	Light Pen (Low)	Pointer	r									r								r									
Access ports to the CRTC on CPC			r/w	7	6	5	4	3	2	1	0	r/w	7	6	5	4	3	2	1	0	r/w	7	6	5	4	3	2	1	0
&BC00	Register selection	Number	w									w								w									
&BD00	Register write	Value	w									w								w									
&BE00	Register status	Function										r		L	b					r									
&BF00	Register read	Value	r									r								r									

See Chapters 21, 26.1.8 and 26.1.9 for more information on the content of the status register and reading this register according to the different CRTC's.

4.4 CRTC ACCESS

4.4.1 GENERAL

Access to I/O with a Z80A usually requires the use of specific instructions.

These instructions (OUT, OUTI, INI, IND...) are in principle intended to use devices whose addresses are defined on the least significant 8 bits of the 16-bit address bus.

The 16-bit address bus is specified in the **BC** register, but some instructions (OUTD, OUTI, INI, IND, ...) also use **B** as counter.

From a computer design perspective, it is not advisable to place the address of devices that can use these instructions on the most significant byte of the 16-bits address bus.

This wise advice from Mr. ZILOG was not listened to by Mr. SUGAR.

Also access to devices on CPC mainly goes through **A8..A15 bits of the address bus** (FDC 765 being an exception in part).

Device selection bits should therefore be set to B.

Welcome to the CPC!

Examples		
Selection register 12		
	BASIC	OUT &BC00,12
	Z80A	LD BC,&BC00+12:OUT(C),C
Sending valeur &30 in register 12 (previously selected)		
	BASIC	OUT &BD00,&30
	Z80A	LD BC,&BD30:OUT (C),C
Reading register 12 (previously selected / updated)		
	BASIC	PRINT INP(&BF00)
	Z80A	LD BC,&BF00 : IN A,(C)
Reading status register		
	BASIC	PRINT INP(&BE00)
	Z80A	LD BC,&BE00 : IN A,(C)

The use of register B prevents the use of interesting instructions to send or read a series of successive values on a port, such as OTIR, OTDR, INIR, INDR.

Indeed, these instructions use B as the counter of the number of values to be read in a table and decrement this counter until it reaches the value 0.

Digressive Remark :

These repetitive instructions can be used experimentally, to process more than one value, on a device whose selection bits do not participate in the counter (most significant bits), such as the GATE ARRAY. It is possible to issue one of these instructions and savagely interrupt it by positioning it judiciously before an interruption occurs. This interruption will nevertheless have to "forget" the return address placed on the stack before re-authorizing other interruptions. This interesting aspect is however very limited (and especially playful) and can activate other devices depending on the number of values read in the table.

However, it is still possible to use

- OUTI or OUTD instructions to send one by one the data from a table (pointed by HL) to the CRTC.
- INI or IND instructions to read one by one the data from a table (pointed by HL) of the CRTC.

The advantage is that these instructions are "fast" according to the number of operations performed.

The use of the OUTI/OUTD statement is possible by first incrementing B between each instruction for OUTI/OUTD because B is decremented before accessing the port. For the CRTC, which uses bits 0 and 1 of B as an index, this implies that B is pre-loaded with the port address + 1 for the OUTI/OUTD instructions to work.

For reading instructions, the addressed device is defined by BC before B is decremented, so it must contain the normal address of the port before reading.

Example in Z80A :

```
LD BC,&BC02      ; Hsync position register selection
OUT (C),C
LD HL,TABHSYNC   ; Pointer to Hsync position table
LD B,&BD+1       ; IO Address sending data+ 1 : &BE
OUTI             ; OUTI decrease B by 1, send TABHSYNC[0] on the &BD IO Addr
                ; and then increase the pointer by 1
INC B            ; B is set again to &BE
OUTI            ; OUTI decrease B by 1, send TABHSYNC[1] on the &BD IO Addr
                ; and then increase the pointer by 1
```

TABHSYNC DB 50, 10

4.4.2 Z80A INSTRUCTIONS

Instructions in Z80A for processing Input/Output :

INSTR.	DURATION	DESCRIPTION
OUT (C),r8	4 µsec	r8=[A or B or C or D or E or H or L] Writing to devices defined in BC the value contained in the r8 register.
OUT (n),A	3 µsec	The input-output address is defined by the couple An, and the data sent to the device is A. This double constraint drastically limits the number of values available to one device without causing a collateral effect on another device (selection + value).
OUT (C),0	4 µsec	Writing value 0 to the device(s) defined in BC. An interesting instruction for a demomaker! But not only that...
OUTI	5 µsec	Decrement B, then read the value pointed by HL, incrementing HL and sending the value read on the port sent by BC.
OUTD	5 µsec	Decrement B, then read the value pointed by HL, decrementing HL and sending the value read to the port sent by BC
IN r8,(C)	4 µsec	r8=[A or B or C or D or E or H or L] Read in the r8 register the value sent by the device defined in BC. If several devices are selected, there is no doubt that a game of musical chairs will take place...
IN A,(n)	3 µsec	The input-output address is defined by the couple An, and the data read will modify A.
IN (C)	4 µsec	It is an "unofficial" instruction. The value present on the data bus is read and its evaluation affects F.
INI	5 µsec	Reading the value on the port addressed by BC and writing this value to the address pointed by HL, HL decrement, B decrement
IND	5 µsec	Reading the value on the port addressed by BC and writing this value to the address pointed by HL, HL decrement, B decrement

4.4.3 ACCESS DELAYS

The following table indicates for some I/O write instructions the timing of the register update in the CRTC and for some I/O read instructions the timing when the value from the circuit is updated in the Z80A register or RAM.

INSTRUCTIONS	DURATION	I/O CONSIDERATION	
		CRTC 0, 1, 2	CRTC 3, 4
OUT (C),r8	4 μ sec	3rd μ sec	4th μ sec
OUT (C),0	4 μ sec	3rd μ sec	4th μ sec
OUT (n),A	3 μ sec	3 rd μ sec	3rd μ sec
OUTI	5 μ sec	5th μ sec	5th μ sec
OUTD	5 μ sec	5th μ sec	5th μ sec
IN r8,(C)	4 μ sec	4th μ sec	4th μ sec
INI	5 μ sec	4th μ sec	
IND	5 μ sec	4th μ sec	
IN A,(n)	3 μ sec	3rd μ sec	3rd μ sec

It is important to note however, that consideration of a write during the update microsecond does not take place at the same "time" according to the instructions used, and this can therefore affect the management of the value by the circuit.

One way to measure this difference is to use processes that are not "slowed down" by the CRTC and the GATE ARRAY, such as the HSYNC display for example. See Chapter 16, page 133.

We can also measure this difference, for example, between what happens with an I/O on the 3rd NOP of an OUT(C),R8 and the 5th NOP of an OUTI on a CRTC 1. See Chapter 13.6.2, page 109.

It should also be noted that on CRTC's 3 and 4, the CRTC misses the I/O on the 3rd μ sec of OUT(C),R8 instruction and retrieves it on the 4th μ sec of the instruction. Which delays register updates by 1 μ sec if this instruction is used. **This shift does not occur if the OUTI/OUTD instructions are used.** See next Chapter.

The majority of the diagrams that refer to Input-Outputs in this document are performed on the basis of the OUT(C),R8 instruction. For CRTC's 3 and 4, the Input-Output is positioned on the 4th μ second.

In practice, for code produced for CRTC's 3 or 4, it is necessary to position a write I/O instruction 1 μ sec before the one which would have been placed for CRTC's 0, 1 or 2.

This is established!

4.4.4 OUTs DISSECTION

This chapter aims to try to explain why an output entry with an "OUT(C),R8" occurs on the 3rd NOP for a CRTC equipped with a GATE ARRAY, and on the 4th NOP for an ASIC that emulates a CRTC (CRTC's 3 and 4), but also why there is a difference (whether on a CRTC or ASIC) between an input/output performed with an "OUT(C),R8" and that performed with an "OUTI".

The GATE ARRAY, within the CPC, is THE conductor for many components. It is clocked at the staggering speed of 16 MHz (which allows it to display pixels Mode 2 at 0.0625 μ Sec). It gives a 1 MHz rate for the AY-3-8912 (sound generator), the CRTC, and clocks the Z80A at 4 MHz.

One of the objectives of the gate array designers was to use Z80A's ability to slow down its execution to retrieve the RAM access priority for addresses pointed to by the CRTC.

The instructions of a z80a consist of periods of execution (called cycles M) in which several sub-periods occur (called cycles T). Each "T" sub-period duration is 0.25 μ sec (the size of 4 pixels in graphic mode 2).

The common point of all Z80A instructions is the need to access the RAM to read the code(s) of the instruction to be executed (called "**opcode**" for operation code). This reading, called "**opcode fetch**", is performed during a first cycle called M1. Each cycle M performs a basic instruction :

- Reading a RAM opcode ("opcode fetch").
- Reading or writing in a byte by the Z80A internal code that executes the opcode.
- Reading or writing an input / output port ("IO REQ").
- Bus: request or acknowledge.
- Interruption: request or acknowledge.

A cycle M consists of several T cycles, some of which place a wait signal in the active state to indicate to another circuit that the Z80A agrees that it should be slowed down. This wait cycle is commonly named **Tw**. This is particularly the case for the instructions:

- OPCODE FETCH, during the **2nd cycle T**.
- Reading or writing memory, during the **2nd cycle T**.
- IO REQ, during the **3rd cycle T**.

When the Z80A "performs" a cycle Tw, it looks at its Wait line (in this case that connected to the gate array) and if it is active, then it will generate another cycle TW.

This makes it possible to block the processor indefinitely if the circuit that drives the line wait decides to.

This blocking is only possible if the processor has allowed it in a **Tw** cycle and the GATE ARRAY/ASIC made the blocking request at that time.

The trick of the **GATE ARRAY/ASIC** designers has been to **continually generate 3 Tw followed by a "no Tw" cycle**. When the Z80A, for a Cycle T that makes a wait, falls on one of these cycles Tw, it will run the "remaining" sequence of Tw, which has the effect of "**linearizing**" the instructions over 4 T Cycles.

In other words, if an instruction started on an "aligned" T-cycle and ends with a number of T-cycles which is not a multiple of 4, then the next instruction will be "stretched" during its first cycle "M".

To illustrate this, diagram A on the following pages describe an **OUT(#nn),A** instruction (1 opcode #D3) that needs 11 cycles to run. This instruction has an odd number of T-cycles (so no multiple of 4) and is immediately followed by a second **OUT (#nn),A**.

When running the first **OUT(#nn),A**, none of the WAIT signals of the Z80A falls at the same time as a WAIT signal from GATE ARRAY. The instruction is executed in 11 T-Cycles ($0.25 \times 11 = 2.75$ μ Sec).

When the second **OUT(#nn), A** is executed, the WAIT signal from the Z80A during cycle M1 occurs at the same time as the WAIT signal from the GATE ARRAY. This causes the generation of a 2nd wait T-cycle by the Z80a (see "**Wait extent**" on the diagram A). During this 2nd wait cycle, the GATE ARRAY does not send a WAIT signal, which stops the generation of wait cycles by the z80a. Therefore this 2nd OUT (#nn), finds itself "stretched" by 0.25 μ sec to match the memory access pattern defined by the gate array. Its execution then takes 3 μ sec (12 t-cycles).

And so on. As long as the "rectified" instruction itself contains an "unaligned" number of T-cycles, the duration of the following instruction will also be rectified. Thus in the previous example, if a NOP (4 t-cycles) is added behind the 2nd **OUT(#nn),A**, then the cycle T2 of the M1 cycle will generate a wait at the same time as the gate array, which will lengthen the NOP duration of 0.25 μ sec (so 1.25 μ sec in total). Another NOP after this first NOP will be aligned. Indeed, the T2 cycle of its M1 cycle will be aligned with the "non-wait cycle" of the GATE ARRAY, and the instruction will then run in 4 T-Cycles (1 μ sec).

The same goes for all the instructions whose M1 cycle lengthens according to the timing of the gate array in order to maintain priority on the RAM accesses to the address provided by the CRTC every 4 T-Cycles.

As part of an I/O writing operation, this mechanism is used to stall, compared to the beginning of a μ sec, the moment when I/O begins. In this case on **the cycle T2 of the I/O M cycle**. The Z80A puts the I/O address on the data bus (a reminder of address &BD00 for writing to a CRTC register).

The GATE ARRAY clocks the CRTC at 1 MHz (but not quite at the same time as for the AY-3-8912). The CRTC periodically checks whether the Z80A IORQ signal is active in order to determine if it is affected by the I/O. If this is the case when writing, it can recover the value to select one of its registers or update the one that is selected.

Depending on the instruction which generates the I/O, the data is not immediately present when the CRTC is in a state to update its registers, which may have the consequence of deferring the writing of registers between 2 different instructions within the same micro-second. This is particularly the case between the instruction OUT(C),reg and OUTI, whose difference can be highlighted with R2.jit or R3.jit techniques, for example. Diagram B on the following pages parallels these two instructions.

In principle, the ASIC's do not clock the CRTC exactly like the GATE ARRAY ("CRTC's" 3 and 4). There is undoubtedly a lag of the type which I represented on diagram C, which has the consequence of modifying the time of register updates relative to what happens with the GATE ARRAY.

It also explains why the update of a CRTC register takes place on the 5th μ sec of the OUTI instruction, regardless of the type of CRTC, while there is a difference of 1 μ sec when the update takes place with the OUT(C),R8 instruction.

Diagram A : OUT(#NN),a + OUT (#nn),A + NOP + NOP

OUT(#nn),A		1 μSec														1 μSec														1 μSec															
GA	1	WAIT				WAIT				WAIT				WAIT				WAIT				WAIT				WAIT																			
Z80 Cycle M		M1 - FETCH 0xD3														M2 - READ CYCLE														M3 - OUT															
No Tcycle		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
Z80A Oper		--				MREQ RD				RFSH				RFSH MREQ				--				MREQ RD				MREQ RD				--				WR IORQ				WR IORQ				WR IORQ			
Z80A Tw		WAIT				WAIT				WAIT				WAIT				WAIT				WAIT				WAIT																			

OUT(#nn),A		1 μSec														1 μSec														1 μSec															
GA	2	WAIT				WAIT				WAIT				WAIT				WAIT				WAIT				WAIT																			
Z80 Cycle M		M1 - FETCH 0xD3														M2 - READ CYCLE														M3 - OUT															
No Tcycle		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
Z80A Oper		--				MREQ RD				RFSH				RFSH MREQ				--				MREQ RD				MREQ RD				--				WR IORQ				WR IORQ				WR IORQ			
Z80A Tw		WAIT				WAIT extent				WAIT				WAIT				WAIT				WAIT				WAIT																			

NOP		1 μSec														1 μSec																					
GA	3	WAIT				WAIT				WAIT				WAIT				WAIT				WAIT															
Z80 Cycle M		M1 - FETCH 0x00														M1 - FETCH 0x00																					
No Tcycle		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7	8	9	10	11
Z80A Oper		--				MREQ RD				RFSH				RFSH MREQ				--				MREQ RD				RFSH				RFSH MREQ							
Z80A Tw		WAIT				WAIT extent				WAIT				WAIT				WAIT				WAIT															

Diagram B : OUT(C),H vs OUTI on CRTC 0, 1, 2

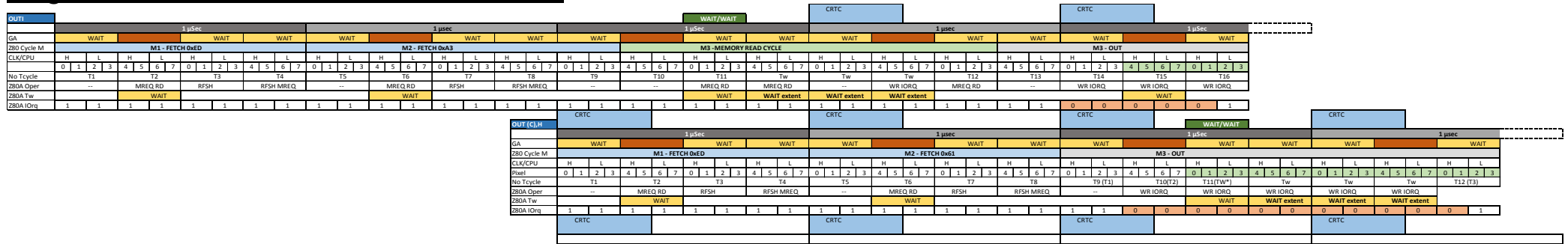
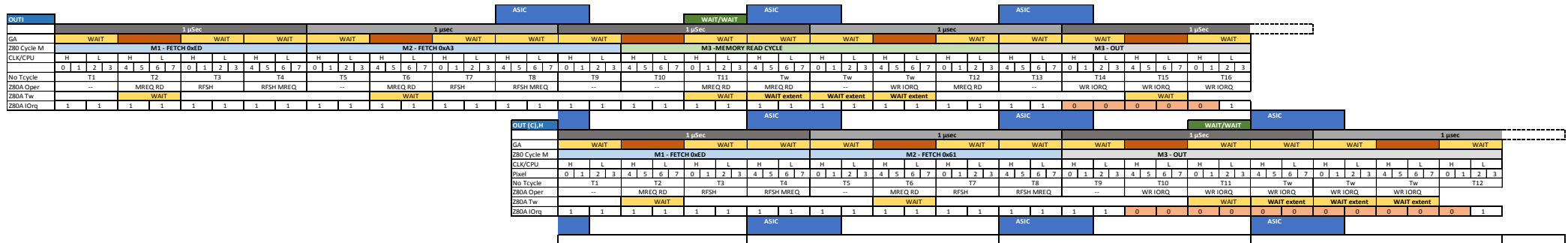


Diagram C : OUT(C),H vs OUTI on CRTC 3, 4



5 OTHER CIRCUITS

5.1 ACCESS

The devices on the CPC are wired in such a way as to partially decode the address used to perform the Input/Output. (Did I ever write "Welcome to CPC"?).

A device is affected by an Input/Output operation as soon as a few precise bits of the address bus are set to 0 and/or 1. This implies that if other bits relative to other devices are also set, then the Input/Output operation will also affect them.

It is therefore possible to send the same value to different devices **simultaneously**.

The advantage may seem relative because the common values useful to several devices are not huge. However, if we measure the consequences of sending unforeseen values to a device, it makes it possible to make "savings" of register(s) by judiciously modifying the value of the Z80A B and/or C registers.

In an environment highly constrained by machine time, it may have the advantage of assigning other uses to these registers.

Circuit	r/w	Register B (or A)								Register C (or n)								Select Addr
		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
PAL	w	0	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	&7F00
Gate Array	w	0	1	x	x	x	x	x	x	x	x	x	x	x	x	x	x	&7F00
CRTC Select	w	x	0	x	x	x	x	0	0	x	x	x	x	x	x	x	x	&BC00
CRTC Write	w	x	0	x	x	x	x	0	1	x	x	x	x	x	x	x	x	&BD00
CRTC Status	r	x	0	x	x	x	x	1	0	x	x	x	x	x	x	x	x	&BE00
CRTC Read	r	x	0	x	x	x	x	1	1	x	x	x	x	x	x	x	x	&BF00
ROM Select	w	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	x	&DF00
Printer	w	x	x	x	0	x	x	x	x	x	x	x	x	x	x	x	x	&EF00
PPI Port A	r/w	x	x	x	x	0	x	0	0	x	x	x	x	x	x	x	x	&F400
PPI Port B	r/w	x	x	x	x	0	x	0	1	x	x	x	x	x	x	x	x	&F500
PPI Port C	r/w	x	x	x	x	0	x	1	0	x	x	x	x	x	x	x	x	&F600
PPI Control	w	x	x	x	x	0	x	1	1	x	x	x	x	x	x	x	x	&F700
FDC Status	r	x	x	x	x	x	0	x	1	0	x	x	x	x	x	x	0	&FB7E
FDC Data	r/w	x	x	x	x	x	0	x	1	0	x	x	x	x	x	x	1	&FB7F
FDC Motor	w	x	x	x	x	x	0	x	0	0	x	x	x	x	x	x	x	&FA7F

Finally, still from the perspective of constrained environments, it may be useful to consider that not all bits of a value sent to a device are useful.

For a CRTC, this is true for register update data, such as R9 truncated to 5 bits, as well as the value of the register number.

In other words, you can select R9 with the value 9, but also &31 (00110001), and update it with the value 7, but also &27 (00100111).

5.2 CPC + / GX 4000

On the AMSTRAD PLUS, it is possible to communicate directly with the emulated CRTC, via additional registers created specifically to manage the complementary "PLUS" functions. These functions allow for example, the masking of data, performing fine shifts, defining lines and addresses of rapture, or even to stall a raster or "DMA" interrupt (not without bugs however!).

The current objective of this document is not (yet) to analyse the interaction between these registers and the EMULATION of the CRTC. Access to these specific registers does not pass through the Z80A's input/output system described above.

The AMSTRAD PLUS has a page of registers "mapped" on a memory area.

Each register therefore has its own address.

The Z80A accesses these registers with simple writes (or reads) to a given address.

It is therefore possible to access certain functions (e.g. changing colours) in two different ways. The information provided for CRTC 3 in this version of the document relates only to I/O performed via the Z80A OUT Instructions.

It should be noted, however, that the page of these registers, located between &4000 and &7FFF, is accessible via a previously untapped function of the GATE ARRAY.

However, this function itself is conditional on the use of a 17-byte "unlock" sequence which must be sent to the CRTC's selection port (&BC00) :

255, 0, 255, 119, 179, 81, 168, 212, 98, 57, 156, 70, 43, 21, 138, 205, 238

Remark :

There is no point in sending this unlock sequence to a CRTC 4.

They didn't use the same sequence.

I wouldn't say anything more without the presence of my lawyer.

6 BUILDING A SCREEN

6.1 GENERAL LOGIC

The following algorithms describe the general display management logic of an "ideal" CRT. As we will see later, this logic is sometimes very different depending on the situation.

6.1.1 CHARACTER COUNTING

C0 is incremented by 1

When C0 reaches R0

 C0 goes to 0

 C9 is incremented by 1

 When C9 reaches R9

 C9 goes to 0

 C4 is incremented by 1

 When C4 reaches R4

 When C5 reaches R5

 C4 goes to 0, C5 goes to 0

 MA is updated from R12/R13

 Otherwise C5 is incremented by 1

6.1.2 SYNCHRONIZATIONS

When C0 reaches R2

 Hsync starts, C3h=0

 C3h is incremented if R3h>0

 When C3h=R3h

 End of Hsync

When C4 reaches R7

 Vsync starts, C3v=0

 C3v is incremented

 When C3v reaches R3v (or 16)

 End of Vsync

6.1.3 CHARACTER DISPLAY

When C0 goes to 0

 Character display is enabled

When C0 reaches R1

 Character display is disabled

When C4 goes to 0

 Character line display is enabled

When C4 reaches R6

 Character line display is disabled

6.1.4 VIDEO POINTER

At each μsec , VMA is incremented by 2 as long as the display is active and C9 is part of the address

```

If C0=R0      then C0=0      true for R0=0
                If C9=R9      then C9=0      true for R9=0
                                If C4=R4      then
                                    If R5=0      then      true for R5=0
                                        C4=0      true for R4=0
                                        MA=R12/R13
                                    else C4=C4+1 (CRTC's 0, 1 and 2) and C5 management
                                Else C4=C4+1
                            Else C9=C9+1
Else C0=C0+1
    
```

6.1.5 DIAGRAMS

The following diagrams describe the overall construction of a screen from the different registers, without modifying the registers during the frame.

Screen definitior	Horiz. Reg				Vertical Reg					Vid Ptr		Special
	R0	R1	R2	R3	R4	R5	R6	R7	R9	R12/R13		R8
	63	40	46	14	35	24	25	30	7	&30	0	0

$$(R0+1) \times [((R4+1) \times (R9+1)) + R5]$$

$$64 \times ((36 \times 8) + 24) = 19968 \mu\text{s}$$

Description of the first 16 lines shown in green on the diagrams on the following pages:

Video Pointer																
15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
R12		C9 (*)			R12/13										0	Hex
5	4	2	1	0	9	8	7	6	5	4	3	2	1	0	0	Addr
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	C000
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	C800
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	D000
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	D800
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	E000
1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	E800
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	F000
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	F800
1	1	0	0	0	0	0	0	0	1	0	1	0	0	0	0	C050
1	1	0	0	1	0	0	0	0	1	0	1	0	0	0	0	C850
1	1	0	1	0	0	0	0	0	1	0	1	0	0	0	0	D050
1	1	0	1	1	0	0	0	0	1	0	1	0	0	0	0	D850
1	1	1	0	0	0	0	0	0	1	0	1	0	0	0	0	E050
1	1	1	0	1	0	0	0	0	1	0	1	0	0	0	0	E850
1	1	1	1	0	0	0	0	0	1	0	1	0	0	0	0	F050
1	1	1	1	1	0	0	0	0	1	0	1	0	0	0	0	F850

C9	First byte								Second byte								C4
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	
0																	0
1																	0
2																	0
3																	0
4																	0
5																	0
6																	0
7																	0
0																	1
1																	1
2																	1
3																	1
4																	1
5																	1
6																	1
7																	1

(*) C5 on CRTC 3, 4 in vertical adjustment period (R5)

																																									HSYNC						Latency in Hsync-GA																				
																																									R1						R2														R3			R0			
																																															1 2 3 4 5 6 7 8 9 10 11 12 13 14																				
R12/13	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63			
	0	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	1	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	2	Black																																							DISP-EN Off						Purple																	DISP-EN On			
	3	Black																																							DISP-EN Off						Purple																	DISP-EN On			
	4	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	5	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	6	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	7	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	8	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	9	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	10	Red																																							DISP-EN Off						Purple																	DISP-EN On			
	11	Black																																							DISP-EN Off						Purple																	DISP-EN On			
	12	Black																																							DISP-EN Off						Purple																	DISP-EN On			
	13	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	14	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	15	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	16	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	17	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	18	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	19	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	20	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	21	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	22	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	23	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
	24	Blue																																							DISP-EN Off						Purple																	DISP-EN On			
R6	25	DISP-EN off																																																																	
	26	Yellow																																																																	
	27	Yellow																																																																	
	28	Yellow																																																																	
	29	Yellow																																																																	
R7	30	Vsync																																																																	
R3	31	Vsync																																																																	
	32	Yellow																																																																	
	33	Yellow																																																																	
	34	Yellow																																																																	
R4	35	Yellow																																																																	
R5	35	Yellow																																																																	
		DISP-EN on																																																																	

7 SYNCHRONIZATION

7.1 PRINCIPLES

The CRTC is responsible for determining the memory addresses to be displayed, which it communicates to the GATE ARRAY, which reads the data and manages it according to its parameters, to generate colourful and various width pixel sizes.

The CRTC also sends VSYNC and HSYNC signals to GATE ARRAY, which combines them to send a composite signal to the monitor.

- When the GATE ARRAY receives an HSYNC signal, there is 2 μs of latency before the "real" horizontal synchronisation of the monitor begins.
- When the GATE ARRAY receives a VSYNC signal, there are 2 latency lines before the "true" vertical synchronisation of the monitor begins.

On a topic that deals with the differences between microsecond scale circuit models, it is important to spatialize the instructions in relation to what is displayed.

Several difficulties are associated with this approach:

- Situate a Z80A instruction in relation to the internal workings of the CRTC, as delays may exist between the update of internal records and the time when characters are displayed.
- Determine when, during an Input-Output instruction, the modification of a CRTC register is effective and considered.

The same type of issue exists for Z80A instructions accessing the GATE ARRAY directly, or when updating the RAM read by the GATE ARRAY.

To "synchronize" the instructions, this document uses a single point of reference to which the instructions of the Z80A affecting the video are aligned.

This reference point is the moment when C0 is considered equal to 0 from the perspective of the CRTC.

There is a delay in display between when the CRTC provides a video pointer, and when the GATE ARRAY displays the corresponding 16-bit character.

This delay is 1 μsec .

This display time lag of the GATE ARRAY with respect to the CRTC would not be a problem if the entirety of what is sent by the CRTC to the GATE ARRAY were **always** delayed by 1 μsec .

But this is not always the case, especially for HSYNC signal management for machines equipped with CRTC's 0, 1 and 2.

When this document deals with Z80A instructions, and their synchronization is important with respect to timing differences, that the C0 counter is presented on 2 "time-line". The one with respect to C0 from the CRTC reference point and the one with respect to the display (pixels, ...) by the GATE ARRAY.

It will therefore be a question of "**C0 from Vsync**" (or **C0vs**) and/or "C0 from GA" when the assignment of the CRTC's registers is decisive in relation to the display of characters by the GATE ARRAY.

The CRTC communicates with Z80A in two different ways (outside of the CRTC 1 read or status registers):

- Via the CRTC VSYNC pin that is connected directly to the 0 bit of port B of PPI 8255.
- Via the Z80A interrupts produced by the GATE ARRAY from the CRTC's HSYNC signals.

7.2 VSYNC SYNCHRONIZATION

The CRTC generates a signal on its VSYNC pin one μsec before $C4=R7$ and $C0$ changes to 0. This is a reliable indicator to then base any other synchronization method.

The bit 0 of port B of the PPI ("standard" &F5 input-output address) changes to 1 as soon as the VSYNC signal is produced by the CRTC.

In general, programs make "loops" to wait for this bit to go to 1, which leads to a margin of error related to the duration of the instructions of the waiting code.

This margin exists even if the "loops" code is "aligned" through an interrupt generated from a HALT statement located before the waiting loop (the margin is then just "stable").

However, it is perfectly possible to write code capable of setting Z80A code to the microsecond that corresponds to $C4=R7$ and $C0=C9=0$.

All data shown in this document will use this **COvs** reference point. It is of course possible to use the interrupt system as a new reference point.

Chapter 25.6.6 summarizes interruptions according to the different CRTC's.

It should not be forgotten that interruptions are dependent on the differences between the CRTC/GATE ARRAY couples of the different machines.

The principle of the **COvs** synchronization code is to place a VSYNC wait in a period where the indicator at the PPI level is not yet set to 1.

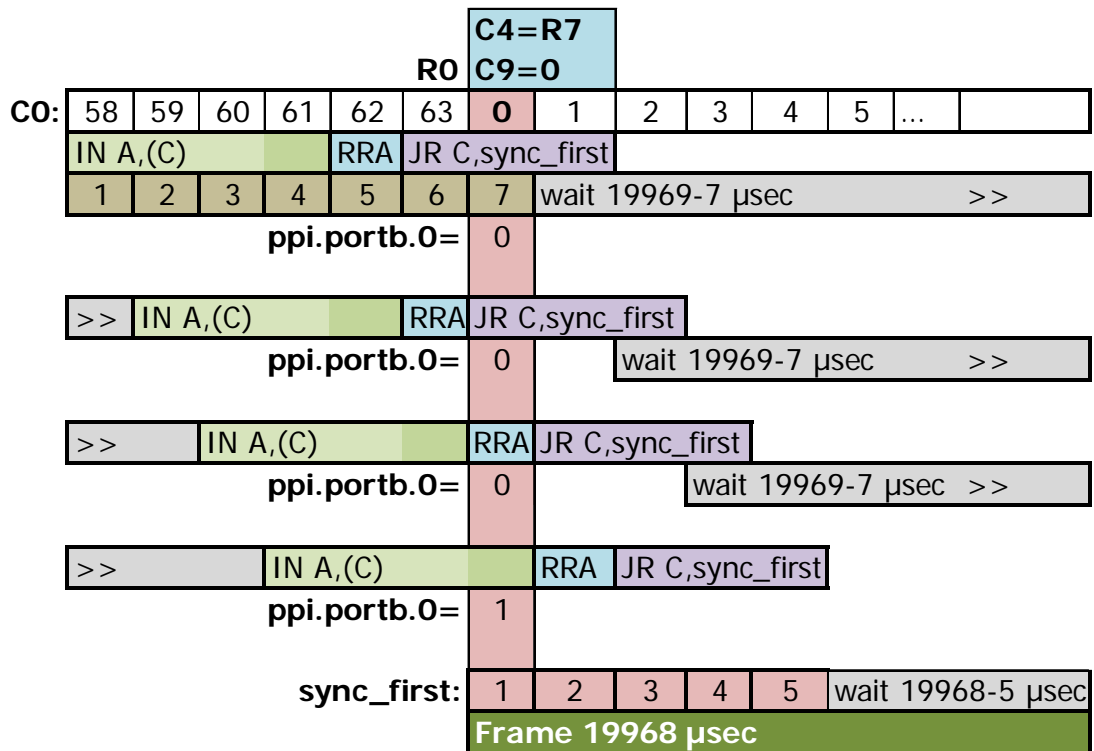
It is then a question of deriving this microsecond code by microsecond at each frame, thanks to a period of **19969** microseconds. This scan is 1 microsecond longer than that produced by the CRTC (with adequate and standard programming of 312 lines of 64 μsec).

This can be seen as a "drift" of the code microsecond-by-microsecond.

The Input-Output instruction, which reads port B of the PPI, is the IN A,(C) instruction and runs in 4 μsec . It is on the 4th μsec of the IN A,(C) instruction that A is updated when the bit 0 of port B changes to 1.

The COvs reference point is calculated in this way and all the information given in this document is correlated with this measurement, which is a single reference point.

Schematic description of this principle :



Synchronisation code :

```

=====
;
; Vsync synchronization
; At the end of the synchronization call, the 1st usec is the one on which the CRTIC has positioned the Vsync signal
; Principle
; - wait for the vsync signal with the margin of error
; - wait for the vsync signal to finish
; - derive the vsync test with a loop during 19968+1 us
; - as soon as the vsync is detected by the test, it is necessary to subtract the duration of the test
;
=====
sync_vbl
    di
    ld b,#f5          ; Wait VBL flag =1
    ld hl,19968-23   ; Nop counter (minus margins and wait management)
    ld de,-11
sync_wvblon1        ; Here we are waiting for the beginning of the VBL period (or we are not waiting if we were there already)
    in a,(c)
    rra
    jr nc,sync_wvblon1
sync_wvbloff1       ; Flag Vsync CRT goes to 1 (or was already to 1)
    in a,(c)         ; Wait for the flag to go back to 0 (End of Vsync)
    rra
    jr c,sync_wvbloff1
sync_wvblon2        ; We are now certain that the Vsync signal was not already in progress
    in a,(c)
    rra              ; margin1 of 7us
    jr nc,sync_wvblon2
sync_wvbloff2       ; Wait for the Vsync signal to return to 0 by counting the time elapsed
    add hl,de        ; 3      On nop2      On nop3
    in a,(c)         ; 4      2              1
    rra              ; 1      1              1
    jr c,sync_wvbloff2 ; 3/2    2              3      (bcl)+3+4+1+2=15 / margin 15-5=10
    ex de,hl        ; 1
    call wait_usec   ; 5 >> 6 + 10(margin2)
    ;
    ; Drift zone to wait again for the first manifestation of the flag
    ; the in a,(c) will "go down" nop by nop (frame by frame) until the in recovers the active flag
sync_derive_bcl
    ld b,#f5          ; 2

```

```

in a,(c) ; 4 usec. 0.1.2.[3] (+1)
rra ; 1 usec (+1)
jr c, sync_first ; 2/3 (+3)
ld de, 19969-20 ; 3
call wait_usec ; 5+ (19969-20)
jr sync_derive_bcl ; 3 >> 20
sync_first ; 6 The flag has been detected at the earliest, and this since 5 usec (2+1+3) C0=R0
; -1 µs to position on C0=0
ld de, 19968-11 ; 3
jp wait_usec ; 3 >> 11 >> de=19968-11

```

```

;=====
; wait "de" usec
; 40+(((de/8)-5) x 8)+(de and 7) nop
; nb - the call of the function is not included
;=====

```

```

wait_usec:
ld hl, sync_adjust ; 3
ld b, 0 ; 2
ld a, e ; 1
and %111 ; 2>8
ld c, a ; 1
sbc hl, bc ; 4
srl d ; 2
rr e ; 2>17
srl d ; 2
rr e ; 2
srl d ; 2
rr e ; 2>25
dec de ; 2>27 8
dec de ; 2>29 16
dec de ; 2>31 24
dec de ; 2>33 32
dec de ; 2>35 40 *
nop ; 1>36

wait_usec_01
dec de ; 2 -
ld a, d ; 1 -
or e ; 1 -
nop ; 1 -
jp nz, wait_usec_01 ; 3 - v=(8 x DE)
jp (hl) ; 1>37
nop ; 1 * v=0--7
nop ; 1
nop ; 1
nop ; 1
nop ; 1
nop ; 1
nop ; 1

sync_adjust
ret ; 3>40 *

```

7.3 FAKE VSYNC

The VSYNC signal is part of a tripartite relationship between the CRTIC, GATE ARRAY and PPI. CRTIC reports status of VSYNC pin to PPI and GATE ARRAY.

The PPI 8255 is a programmable generic device interfacing circuit.

AMSTRAD used 3 different versions of this component:

- NEC D8255AC-5
- NEC D8255AC-2
- TOSHIBA TMP8255AP-5

The last digit indicated is the maximum frequency of the circuit. To my knowledge there is no relevant test to differentiate these models.

It is possible to operate the communication pins of this circuit as input or output according to appropriate programming.

Port B of the PPI is designed on the CPC to work as input, and therefore receive information from the devices to which it is connected. It is possible to reprogram this port as output, by setting to 0 the bit 1 of the control register of the PPI located at the address of I/O #F700. Writing to port B (#F500) a value with the bit 0=1 will therefore put pin 25 of the circuit in the high state. This means that the PPI will send its signal to the CRTIC, which in fact will send it back to the GATE ARRAY, since it is also connected to it.

However, I have found, like Kevin Thacker (ArnoldEmu) before me, that this FAKE VSYNC does not work on some CPC's. On other CPC's, the result is incorrect.

On a CRTIC 2, programmed with R2=50 and R3=14, VSYNC is in principle no longer generated.

We will see later that one of the problems with CRTIC 2 is that a GHOST VSYNC is generated if the VSYNC condition takes place during HSYNC. It should therefore theoretically be possible to do this work instead of the CRTIC by placing bit 0 from port B to 1 in the right place and for the right duration.

However, if a PPI-VSYNC is activated for 1024 μ sec instead of the one that would have been generated by the CRTIC, the signal produced by the PPI is not strong enough to counter the low signal generated by a GHOST VSYNC. But when the CRTIC moves its pin back to the low state (when it is already there), then the VSYNC of the PPI is then considered, and the image is stabilized 16 lines higher than expected. An electronics technician would certainly help me to see more clearly.

However, it is still possible to bypass CRTIC 2's GHOST VSYNC more easily, by preventing the VSYNC condition to occur during HSYNC and by updating R7 with C4 right after the end of HSYNC (See Chapter 15.2, page 127).

WARNING : I don't really know the potential "technical" consequences of sending a signal in the opposite direction to the one intended. Having said that, the risk seems quite low since, for several years, many CPC's have contained several CRTIC's welded on top of one another in an orgy of tin. The passive CRTIC(s) then taking signals from the active CRTIC. In the worst case, a CRTIC is worth (still) less than €10.

A bit of history

This is not the first time that an input port has been used as output on the CPC. The older ones will probably remember the download kit which allowed for the retrieval of (paid) programs via a telephone connection connected to the Minitel (I do not know if this system was used with Prestel in U.K.).

The cable of one of these kits was connected from the Minitel socket on the CPC with its JOYSTICK socket, and in order to be able to manage a bidirectional exchange, the keyboard port was then placed in output. Keyboard lines are read through port A of the PPI, via port A of the AY-3-8912 (sound generator).

Even if this had no consequences for the vast majority of users, I witnessed several CPC's whose AY-3-8912 had "permanently lost" part of the bits of some registers of the AY. From memory, it seems to me that these CPCs had particularly high-pitched tones, if it comes to determining which bits were "ravaged".

8 DISPLAY, Z80A & GATE ARRAY

The following diagrams describe in relation to some video ram update instructions by the Z80A and when this update is considered by the GATE ARRAY/ASIC.

Instructions are localized relative to the CRTC's C0vs reference point.

The RAM reading by the GATE ARRAY/ASIC for data modified by the Z80A is the same for all CPC's.

8.1 INSTRUCTION LD(HL),reg8 (2 μsec)

HL=0000	reg8=#FF																			
C0vs	00	01	02	03	04	05	06	07	08	09										
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Z80A Inst	LD (HL),reg8		NOP	NOP	NOP	NOP	NOP	NOP	LD (HL),#00											
Displayed :	00																			

19968-10 μsec

HL=0001	reg8=#FF																			
C0vs	00	01	02	03	04	05	06	07	08	09										
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Z80A Inst	LD (HL),reg8		NOP	NOP	NOP	NOP	NOP	NOP	LD (HL),#00											
Displayed :	00																			

19968-10 μsec

HL=0002	reg8=#FF																			
C0vs	00	01	02	03	04	05	06	07	08	09										
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Z80A Inst	LD (HL),reg8		NOP	NOP	NOP	NOP	NOP	NOP	LD (HL),#00											
Displayed :	FF																			

19968-10 μsec

HL=0003	reg8=#FF																			
C0vs	00	01	02	03	04	05	06	07	08	09										
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19
Z80A Inst	LD (HL),reg8		NOP	NOP	NOP	NOP	NOP	NOP	LD (HL),#00											
Displayed :	FF																			

19968-10 μsec

8.2 INSTRUCTION LD (aaaa),HL (5 μsec)

aaaa=0004	H=#FF, L=#55																		H'=0, L'=0																	
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																			
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33		
Z80A Inst	LD (aaaa),HL												NOP	NOP	NOP	NOP	NOP	NOP	EXX				Ld (aaaa),HL													
Displayed :	00 00																																			

19968-17 μsec

aaaa=0005	H=#FF, L=#55																		H'=0, L'=0																	
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																			
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33		
Z80A Inst	LD (aaaa),HL												NOP	NOP	NOP	NOP	NOP	NOP	EXX				Ld (aaaa),HL													
Displayed :	00 00																																			

19968-17 μsec

aaaa=0006	H=#FF, L=#55																		H'=0, L'=0																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																					
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33				
Z80A Inst	LD (aaaa),HL												NOP	NOP	NOP	NOP	NOP	NOP	EXX				Ld (aaaa),HL															
Displayed :	55 00		L																																			

19968-17 μsec

aaaa=0007	H=#FF, L=#55																		H'=0, L'=0																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																					
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33				
Z80A Inst	LD (aaaa),HL												NOP	NOP	NOP	NOP	NOP	NOP	EXX				Ld (aaaa),HL															
Displayed :	55 FF		L H																																			

19968-17 μsec

8.3 INSTRUCTION PUSH reg16 (4 µsec)

SP=0004		D=#FF, E=#55														H=0, L=0, aaa=0003																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																		
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
Z80A Inst	PUSH DE							NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	Ld (aaa),HL													
Displayed :																																			

19968-17 µsec

SP=0005		D=#FF, E=#55														H=0, L=0, aaa=0004																		
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																	
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33
Z80A Inst	PUSH DE							NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	Ld (aaa),HL											
Displayed :							00	FF																										

19968-17 µsec

SP=0006		D=#FF, E=#55														H=0, L=0, aaa=0005																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																		
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
Z80A Inst	PUSH DE							NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP
Displayed :							00	FF																											

19968-17 µsec

SP=0007		D=#FF, E=#55														H=0, L=0, aaa=0006																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																		
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
Z80A Inst	PUSH DE							NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP
Displayed :							00	FF																											

19968-17 µsec

SP=0008		D=#FF, E=#55														H=0, L=0, aaa=0007																			
C0vs	00	01	02	03	04	05	06	07	08	09	10	11	12	13	14	15	16																		
Video Ptr	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	
Z80A Inst	PUSH DE							NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP	NOP
Displayed :																																			

19968-17 µsec

9 GATE ARRAY

On the CPC, there are 5 models of identified GATE ARRAY. One of the functions of the circuit is to display the pixels depending on the graphical mode and the colour defined for each ink.

- 40007 models (version 1: Ferranti Matrix ULA20RA023, version 2: Ferranti Matrix ULA16RA023) and 40008 (version 2) are pin compatible. It can be noted that there are different markings of the 40007, also available under 40007-4 or 40007-4x. These models are often mounted with a heatsink spread with thermal paste on motherboards.
- The 40010 model exists under 2 versions (1st version 37aa (Matrix LSI HSG3170) and 2nd version 36aa (matrix LSI HSG3130, 23% smaller)). Thanks to Gérald VINCENT for this information.
- ASIC 40226 is used on the low-cost CPC (CRTC 4).
- ASIC 40489 (CRTC 3) is used on CPC + and GX 4000.

AMSTRAD has created an impressive array of different motherboards. This implies that these 3 components can be found on some 464 and 6128 models. I did not see a motherboard of 664 capable of supporting a 40007/40008. Finally, the component is always mounted on a bracket.

Model	Gate Array Nb capacity	40007	40008	40010
464	1	<input checked="" type="checkbox"/>		
464	2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
664	1			<input checked="" type="checkbox"/>
6128	1	<input checked="" type="checkbox"/>		
6128	1		<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>
6128	2	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>	<input checked="" type="checkbox"/>

Note 1: Chapter 3.2.2 of WEKA binders contain an error. The pins of the 40007 are not compatible with those of the 40008/40010.

Note 2: The models of 6128 with a single location equipped with a 40007 are quite rare (MC0057A motherboards from mid-1988). The gate array is covered with a heat sink.

In general, there is a large amount of 464's equipped with various models.

The 664's are mainly equipped with 40008 and 40010.

The 6128's are mostly equipped with 40010 version 36AA.

Contrary to popular belief, there are many identifiable differences between these components. The 40007/40008 seems to be in advance of 1/16 MHz on the 40010 when it processes the bits of the byte fetched from VRAM.

9.1 PIXELS

The GATE ARRAY/ASIC is responsible for converting the memory read by the CRTC into pixels.

It performs this operation by considering both parameters: the **graphics mode** and the **colour associated** with the pixel to be displayed.

This document is not devoted to the GATE ARRAY in detail, but it should be remembered that the CPC has 4 graphic modes, of which 3 are "official".

The graphic mode determines the horizontal size of a pixel (based on the number of colours that pixel can take).

A pixel can be encoded on 1, 2 or 4 bits.

A pixel occupying 1 bit is the finest resolution that GATE ARRAY can produce.

Mode	VRAM BYTE								Displayed Pixels								Definition
0	A0	B0	A2	B2	A1	B1	A3	B3	A3	A2	A1	A0	B3	B2	B1	B0	2 pixels (16 colors)
1	A0	B0	C0	D0	A1	B1	C1	D1	A1	A0	B1	B0	C1	C0	D1	D0	4 pixels (4 colors)
2	A0	B0	C0	D0	E0	F0	G0	H0	A0	B0	C0	D0	E0	F0	G0	H0	8 pixels (2 colors)
3	A0	B0	x	x	A1	B1	x	x	0	0	A1	A0	0	0	B1	B0	2 pixels (4 colors)
Bit Nb:	7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	

A 17th colour, stored in the GATE ARRAY, is displayed when BORDER is activated

This pixel coding represents an index in a table containing 5-bit colour-coded colours.

				INKR			COLOUR				
Colour Index				7	6	5	4	3	2	1	0
0	0	0	0	0	1	0	C1	C1	C1	C1	C1
0	0	0	1	0	1	0	C2	C2	C2	C2	C2
0	0	1	0	0	1	0	C3	C3	C3	C3	C3
0	0	1	1	0	1	0	C4	C4	C4	C4	C4
0	1	0	0	0	1	0	C5	C5	C5	C5	C5
0	1	0	1	0	1	0	C6	C6	C6	C6	C6
0	1	1	0	0	1	0	C7	C7	C7	C7	C7
0	1	1	1	0	1	0	C8	C8	C8	C8	C8
1	0	0	0	0	1	0	C9	C9	C9	C9	C9
1	0	0	1	0	1	0	C10	C10	C10	C10	C10
1	0	1	0	0	1	0	C11	C11	C11	C11	C11
1	0	1	1	0	1	0	C12	C12	C12	C12	C12
1	1	0	0	0	1	0	C13	C13	C13	C13	C13
1	1	0	1	0	1	0	C14	C14	C14	C14	C14
1	1	1	0	0	1	0	C15	C15	C15	C15	C15
1	1	1	1	0	1	0	C16	C16	C16	C16	C16

When the GATE ARRAY displays its pixels, **it is too "fast" for those of MODE 2.**

Indeed, on gate arrays 40007, 40008, 40010 and ASIC 40226 (CRTC 4), pixels in mode 2 are displayed one pixel earlier than for other graphics modes.

They are displayed in "advance" of 1/16 μ sec (0.0625 μ sec).

In other words, the BORDER "stops" 1 pixel earlier on a line in mode 2 and starts 1 pixel earlier when $C0=R1$ (if you have not changed graphics mode during the line).

Since it is possible to change the graphic mode between each line and/or during a line, this must be considered if it is necessary to align pixels displayed in different graphic modes.

ASIC 40489 of the CPC+ is not affected by this discrepancy.

Whatever the graphic mode on this machine, the pixels are aligned.

9.2 COLOURS

When the colour table (ink colour and border colour) is updated, the consideration of this colour change is different dependent on the CRTC version.

However, the time when the update takes place is the same regardless of the mode.

9.2.1 BORDER AND GRAPHIC MODE 2

On some CPC's, the colour update of the border when the CPC is **in graphical mode 2** can have a visual incidence. Indeed, two pixels from another colour may appear at the beginning and at the end of the μ second where the colour changes.

This problem is linked to a power fault that affects the gate array or the resistors and capacitors that surround it to generate colours, but nevertheless I mention it here as this is an issue on a significant number of CPC's. It does not depend on the CRTC, nor the GA model, the phenomenon which has been observed on one GA 40010 (28818 / 36AA) but not on another of the same reference. Finally, fiddling with the power connector to establish a more direct power contact mechanically causes the parasitic pixels to disappear.

Some "redundant" gate array colours (beyond 27) may have a different effect from their "counterpart" colours in the palette, as the parasitic pixels appear (or not). It is useful to recall here that these colours are not strictly identical to their counterpart in the palette, because of the method of generating the colours of the CPC, based on resistance sets and high impedance.

9.2.2 SPEED OF PROCESSING

The following two pages of diagrams describe how different instructions which update the colour of an ink are processed and how the GATE ARRAY/ASIC takes this into account when displaying its pixels.

This colour on the diagrams indicates which pixels according to the mode are affected by the colour change.

Instructions are calibrated according to **COvs** calculated from the VSYNC reference point.

WARNING :

It should not be forgotten that it is the display of pixels in mode 2 that starts earlier than for other modes. Updating the colour of an ink, on the other hand, is considered in the same way regardless of the graphic mode.

The colour therefore changes on the 2nd pixel of a byte in mode 2, but on the pixels 0 of the bytes processed for the other graphic modes.

CRTC 0, 1, 2 / GATE ARRAY 40010

Z80a instr.	OUTI on Gate Array Port. Value on (HL) is VC (010cccc)																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

Z80a instr.	OUT (C),r8 on Gate Array Port with r8=010cccc, color update in the ink of the vram																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

Z80a instr.	OUT (n),A on Gate Array Port.																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

CRTC 3, 4 / ASIC 40489, 40226

Z80a instr.	OUTI on Gate Array Port. Value on (HL) is VC (010cccc)																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

Z80a instr.	OUT (C),r8 on Gate Array Port with r8=010cccc, color update in the ink of the vram																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

Z80a instr.	OUT (n),A on Gate Array Port.																																																																																																
CD from Vsync	06						07						08						09						10						11																																																																		
CD Disp by GA	05						06						07						08						09						10																																																																		
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 0	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43																																																																									
Pixel Mode 1	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	64	65	66	67	68	69	70	72	72	73	74	75	76	77	78	79	80	81	82	83	84	85	86	87																																																	
Byte Offset (0.5 µsec)	10			11			12			13			14			15			16			17			18			19			20			21																																																															
Pixel Mode 2	80	81	82	83	84	85	86	87	88	89	90	91	92	93	94	95	96	97	98	99	100	101	102	103	104	105	106	107	108	109	110	111	112	113	114	115	116	117	118	119	120	121	122	123	124	125	126	127	128	129	130	131	132	133	134	135	136	137	138	139	140	141	142	143	144	145	146	147	148	149	150	151	152	153	154	155	156	157	158	159	160	161	162	163	164	165	166	167	168	169	170	171	172	173	174	175	176

9.3 GRAPHIC MODE

9.3.1 GENERAL

A HSYNC signal provided by the CRTC is composed of several periods within the GATE ARRAY.

A period, which can be called HSYNC-GA, has a maximum duration capped at 6 μ sec and cannot exceed the value defined in R3.

For all CPCs without exception (CRTC's 0 to 4) **a HSYNC of at least 2 μ sec is required for the graphic mode update.**

The update of the internal register containing the mode is effective on the 3rd μ second of the Z80A instruction of I/O **OUT (C),R8** to the GATE ARRAY

The minimum "latency" period for the GATE ARRAY to generate the HSYNC signal needed by the monitor is 3 μ sec.

If the HSYNC-GA is limited to 2 μ sec (via the CRTC's R3 programming), then **the HSYNC signal is not generated for the monitor.** In this situation, a 2 μ sec HSYNC does not prompt the monitor to give up its guts.

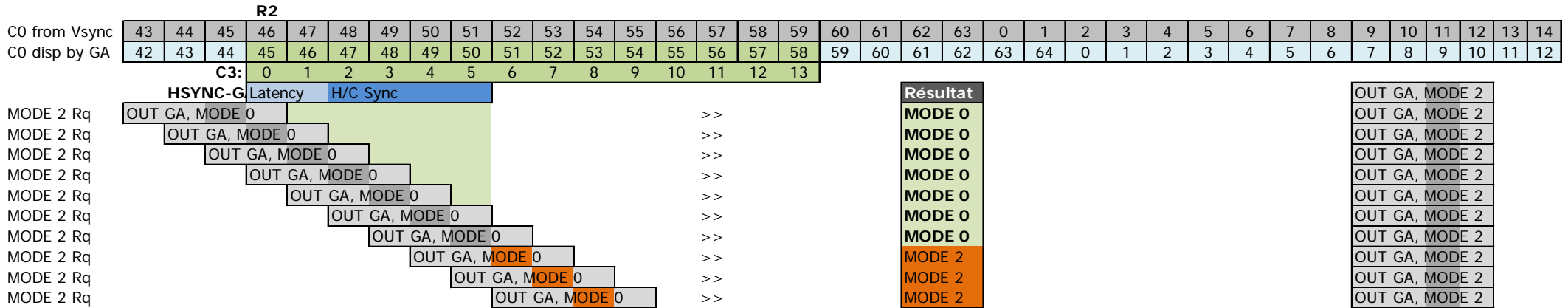
HSYNC is considered more quickly by the GATE ARRAY on CRTC's 0, 1 and 2, than on the ASIC's of CRTC's 3 and 4. ASIC's **delay HSYNC by 1 μ sec, as they do for character display.**

On the VSYNC reference point principle, the following diagrams describe **how a mode change is accounted** for by a Z80A OUT(C),r8 instruction before and during HSYNC.

CRTC 0, 1, 2

CRTC-R2=46

CRTC-R3=14 HBL Size=14 chars

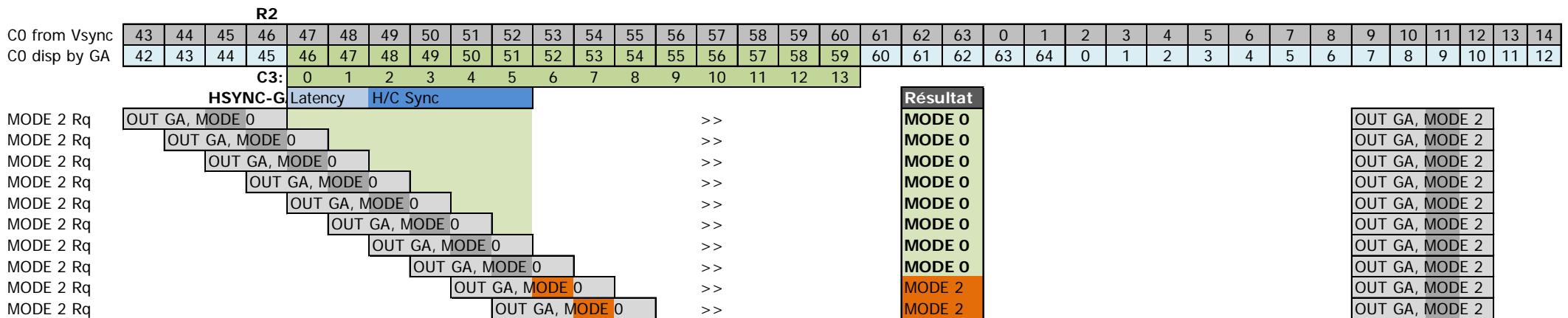


Characters displayed
Hsync "displayed"

CRTC 3, 4

CRTC-R2=46

CRTC-R3=14 HBL Size=14 chars



Characters displayed
Hsync "displayed"

9.3.2 MODE SPLITTING

9.3.2.1 GENERAL

In the following, the **Pixel-M2** terminology designates a pixel whose horizontal size is that of one pixel in graphic mode 2.

A pixel in graphic mode 0 or 3 is composed of **4 Pixel-M2**.

A pixel in graphic mode 1 is composed of **2 Pixel-M2**.

It is possible to change the graphics mode during a line as long as this change of mode precedes an HSYNC programmed with a length $R3 > 1$.

When $R3$ is programmed with the value 2, the change of mode carried out by the GATE ARRAY occurs after the display has been restored on the CRTC's 0, 1, 2 and 4. (to be verified for CRTC 3).

On CRTC's 0, 2 and 4, when the display is reactivated by the GATE ARRAY ($R3=2$), **1 Pixel-M2 is however displayed in the previous graphics mode**. On CRTC 1, the reactivation of the display corresponds exactly to the start of the mode change by the GA, which does not allow you to take advantage of a **nice mode 2 pixel** of the previous graphics mode.

On CRTC's 0, 1 and 2, the GATE ARRAY switches the mode update to the 6th pixel mode 2 (i.e. the 3rd pixel mode 1, the 2nd pixel mode 0).

On the CRTC 4, the GATE ARRAY switches the mode change to the 4th pixel mode 2 (i.e. the 2nd pixel mode 1, the middle of the 1st pixel mode 0).

Given **that mode update occurs during the processing of the byte read in ram**, the algorithm for determining the PEN by the GA switches during processing. Consequently, the calculated PENs are distorted for the rest of the pixels to be displayed in the byte. They are partly composed of the rotations performed for the previous mode.

It is also possible to modify, on CRTC's 0, 1 and 2, the "HSYNC non-display" zone via techniques called **R2.JIT** and **R3.JIT**. (JIT = "Just In Time").

R2.JIT reduces the non-display area of the HSYNC from the left and **R3.JIT** stops the HSYNC 0.25 μsec after its scheduled end. (See Chapters 16 and 14 for more information).

In the context of a graphics mode change, the **R3.JIT** technique does not shorten the period required for the graphics mode update. (You didn't think I wasn't going to try...). Indeed, if this technique is used on the 2nd μsec of the **HSYNC**, the change of graphics mode does not take place. The change of MODE is considered only on an **R3.JIT** during the 3rd μsec . This implies a non-display time of 2.25 μsec for a mode update. This nevertheless has the advantage of moving the moment when a "mixed" mode 2 pixel is visualized in another graphic mode.

The **R3.JIT** is also of great interest insofar as **it allows the modification of the duration of the "official" 4 μsec of the HSYNC monitor with a gap of 0.25 μsec instead of the 0.5 μsec used "classically" to perform horizontal scrolling at byte level.**

The display shutdown delay achieved with **R2.JIT** does not change anything when the display is reactivated, unlike the **R3.JIT**. The GAP between **R2.JIT** and **R2.NJIT** is **3 Pixel-M2 (0.1875 µsec) on CRTC 1** and **4 Pixel-M2 on CRTC's 0 and 2 (0.25 µsec)**.

9.3.2.2 HSYNC UNDER THE MICROSCOPE

The diagrams on the following pages indicate, according to the CRTC's:

- The moment when the display stops when an HSYNC has been requested (with however a tolerance of $\frac{1}{2}$ Pixel-M2 (0.03125 µsec)) using **R2.JIT** or **R2.NJIT**.
- The gap in Pixel-M2 between an **R2.JIT** and **R2.NJIT** technique.
- The moment when the display resumes for **1 Pixel-M2** (area indicated in yellow).
- When the graphics mode changes (shown in pink).
- When the display stops when a **HSYNC** is stopped using **R3.JIT**.

CRTC 0																																																																																																																																																			
R2. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																																																																																																																						
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39																																																																																																											
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
JIT/NJIT GAP										1	2	3	4																																																																																																																																						
R2. NJIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																																																																																																																						
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39																																																																																																											
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
R3. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4							VRAM + 5																																																																																																															
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44																																																																																																						
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19							20							21						
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19							20							21						
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
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CRTC 2																																																																																																																																																			
R2. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																																																																																																																						
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39																																																																																																											
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
JIT/NJIT GAP										1	2	3	4																																																																																																																																						
R2. NJIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																																																																																																																						
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39																																																																																																											
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19																				
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
R3. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4							VRAM + 5																																																																																																															
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44																																																																																																						
MODE 1	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19							20							21						
MODE 0,3	0			1				2							3							4							5							6							7							8							9							10							11							12							13							14							15							16							17							18							19							20							21						
DISPLAY										HSYNC COLORLESS																																						MODE SWITCH																																																																																																			
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CRTC 1																																																					
R2. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																								
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39													
MODE 1	0							1							2							3							4																								
MODE 0,3	0							1							2							3							4							5																	
DISPLAY											HSYNC COLORLESS																		MODE SWITCH																								
JIT/NJIT GAP			1	2	3																																																
R2. NJIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4																								
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39													
MODE 1	0							1							2							3							4							5																	
MODE 0,3	0							1							2							3							4							5							6										
DISPLAY											HSYNC COLORLESS																		MODE SWITCH																								
R3. JIT	VRAM							VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4					VRAM + 5																			
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44								
MODE 1	0							1							2							3							4							5							6										
MODE 0,3	0							1							2							3							4							5							6							7			
DISPLAY											HSYNC COLORLESS																		MODE SWITCH																								

=ALLOWANCE

CRTC 4																																																							
R2. NJIT	VRAM + 1							VRAM + 2							VRAM + 3							VRAM + 4							VRAM + 5							VRAM + 6																			
MODE 2	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40	41	42	43	44	45	46	47							
MODE 1	0							1							2							3							4							5							6												
MODE 0,3	0							1							2							3							4							5							6							7					
DISPLAY											HSYNC COLORLESS																		MODE SWITCH																										

=ALLOWANCE

9.3.2.3 CRTIC 0, 1, 2 : COOKING OF PIXELS WITH R3.NJIT

When the GATE ARRAY switches from one graphics mode to another mode, it is already processing one-byte data according to the previous mode, and result obtained reflects its internal logic.

With **R2.NJIT**, the display stops:

- For 2 μ sec on CRTIC's 0 and 1 (32 Pixel-M2).
- Lasting 2.0625 μ sec on CRTIC 2 (33 Pixel-M2).

With **R2.JIT**, the display stops:

- Lasting 1.75 μ sec on CRTIC 0 (28 Pixel-M2).
- Lasting 1.8125 μ Sec on CRTIC's 1 and 2 (29 Pixel-M2).

On CRTIC's 0 and 2, the display is restored 1 Pixel-M2 before the GATE ARRAY changes the graphics mode. **The 30th Pixel-M2 displayed therefore has the characteristics of the previous mode, for its fraction corresponding to 1 Pixel-M2.**

On CRTIC 1, it should be considered that the "Hsync No Disp" zone indicated on the diagrams is longer by 1 Pixel-M2. The first Pixel-M2 obtained when the display is activated is only displayed for CRTIC's 0, 2 and 4. CRTIC 1 does not display this pixel.

This additional pixel is symbolized in purple on the following diagrams.

There is a notable difference between the GATE ARRAY 40007/40008 and the 40010. Indeed, in certain situations, when bits of the data in VRAM have already been used in the calculation of a colour number of the pixels of the starting mode, these bits are considered to be 0 (GA 40010) or 1 (GA 40008) for the calculation of the new graphic mode colour numbers.

9.3.2.3.1 MODE 2 TO MODE 0.1.2.3

On a line displayed in MODE 2, the data display resumes:

- On CRTIC's 0 and 2, from the **5th Pixel-M2 of the 5th VRAM byte.**
- On CRTIC 1, from the **6th Pixel-M2 of the 5th VRAM byte.**

On CRTIC's 0 and 2, the first pixel displayed is in MODE 2 (PEN 1 or 0).

Since the MODE 2 pixels are "ahead" of the pixels of the other modes, the GATE ARRAY will display **4 new Pixel-M2 after the 5th**, unless the mode has not changed.

This represents the display of 9 M2-pixels from a single byte.

The GATE ARRAY considers that its bit counter is not at 0 but at 5.

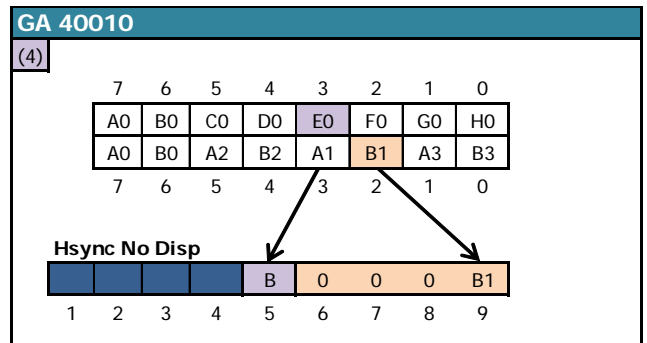
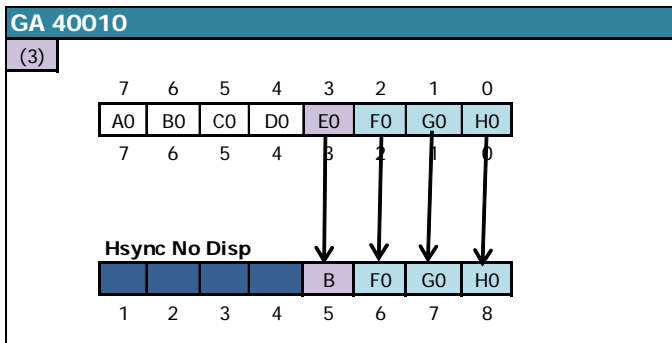
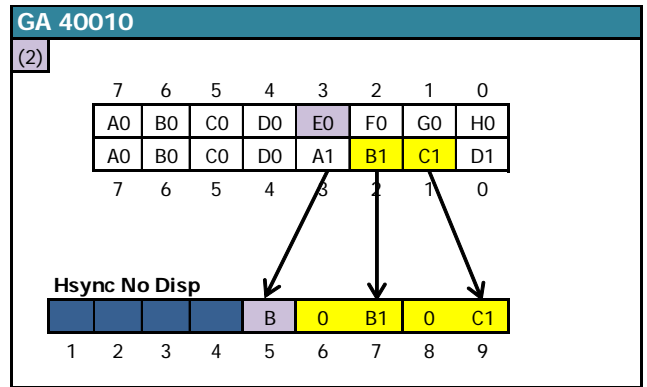
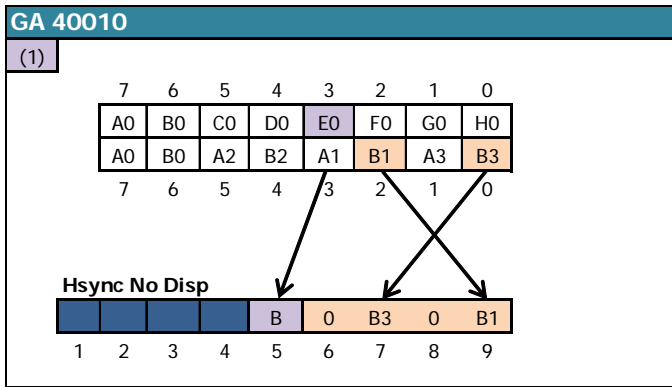
From the 6th bit of the byte read in VRAM, it "starts" processing the calculation of the colour number as if they were the 1st bits of a byte. Thus it considers bits b2,b1 and b0 of the byte in VRAM as those it would have encountered in bits b7,b6 and b5 of this same byte.

Bits missed by the GATE ARRAY 40010 are considered 0, which limits colour number combinations:

- **MODE 2 to MODE 0:** Colour numbers **0, 1, 4, 5**
- **MODE 2 to MODE 1:** Colour numbers **0, 1**
- **MODE 2 to MODE 3:** Colour numbers **0, 1**

The table below describes the interpretation by the GATE ARRAY 40010 of the VRAM byte processed when the redisplay is activated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte								GA 40010 : Displayed Pixels											
2	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(1)	0	b0	0	b2						
2	1	b7	b6	b5	b4	b3	b2	b1	b0		(2)	0	b2	0	b1						
2	2	b7	b6	b5	b4	b3	b2	b1	b0		(3)	b2	b1	b0							
2	3	b7	b6	b5	b4	b3	b2	b1	b0		(4)	0	0	0	b2						
										1	2	3	4	5	6	7	8	9			



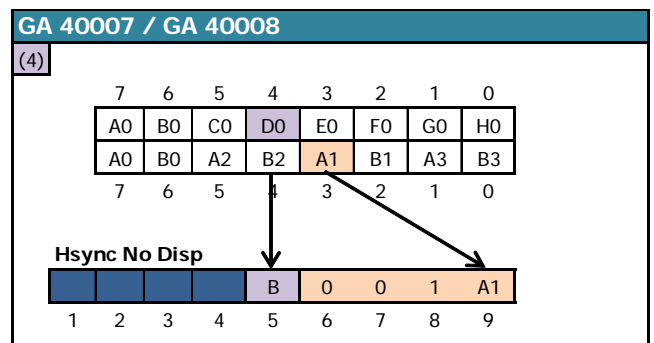
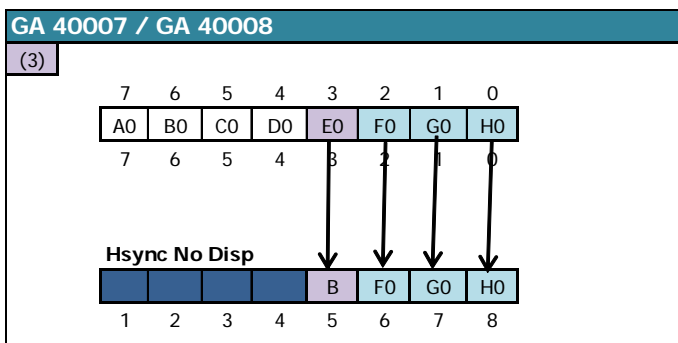
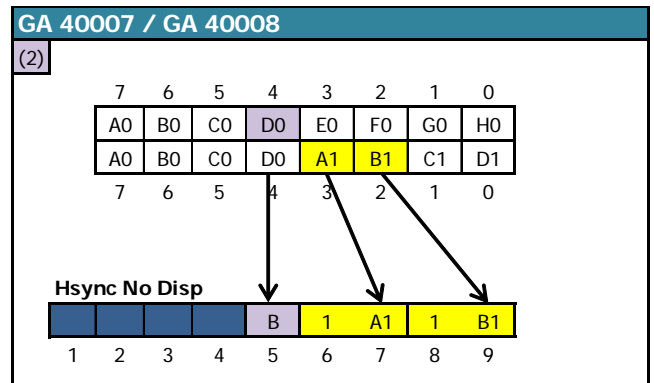
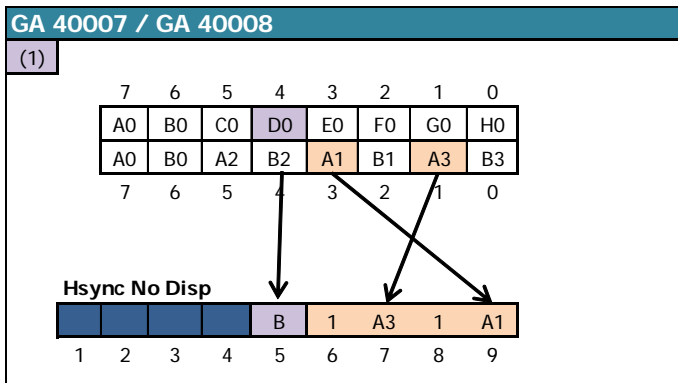
The GATE ARRAY 40007 and 40008 are ahead of 0.0625 µsec compared to the 40010 when they recover the bits allowing for the constitution of the colour number. Missed bits are considered to be 1, which limits colour number combinations:

- **MODE 2 to MODE 0:** Colour numbers 10, 11, 14, 15
- **MODE 2 to MODE 1:** Colour numbers 2, 3
- **MODE 2 to MODE 3:** Colour numbers 2, 3

The table below describes the interpretation by the **GATE ARRAY 40007 and 40008** of the VRAM byte processed when the redisplay is activated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte							
2	0	b7	b6	b5	b4	b3	b2	b1	b0
2	1	b7	b6	b5	b4	b3	b2	b1	b0
2	2	b7	b6	b5	b4	b3	b2	b1	b0
2	3	b7	b6	b5	b4	b3	b2	b1	b0

GA 40007/8 : Displayed Pixels									
Hsync No Disp					(1)	1	b1	1	b3
Hsync No Disp					(2)	1	b3	1	b2
Hsync No Disp					(3)	b2	b1	b0	
Hsync No Disp					(4)	0	0	1	b3
1	2	3	4	5	6	7	8	9	



9.3.2.3.2 MODE 0 TO MODE 0.1.2.3

On a line displayed in MODE 0, the data display resumes:

- On CRTC's 0 and 2, from the **4th Pixel-M2 of the 5th VRAM byte**.
- On CRTC 1, from the **5th Pixel-M2 of the 5th VRAM byte**.

On CRTC's 0 and 2, the first Pixel-M2 displayed is the last of the **4 pixel-M2 of the MODE 0 pixel** displayed in its original colour (i.e. a colour number between 0 and 15). In other words, only ¼ of the MODE 0 pixel is displayed before the GATE ARRAY displays the following pixels.

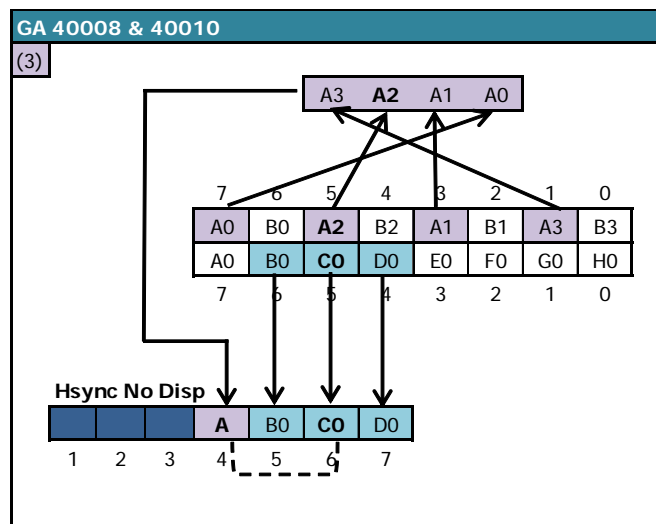
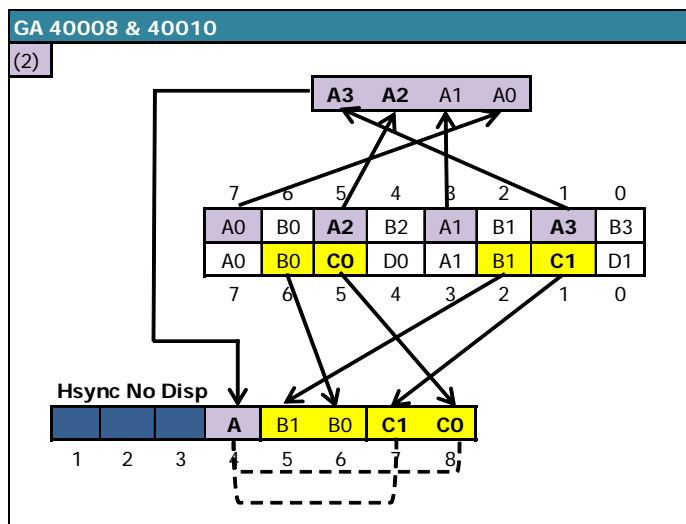
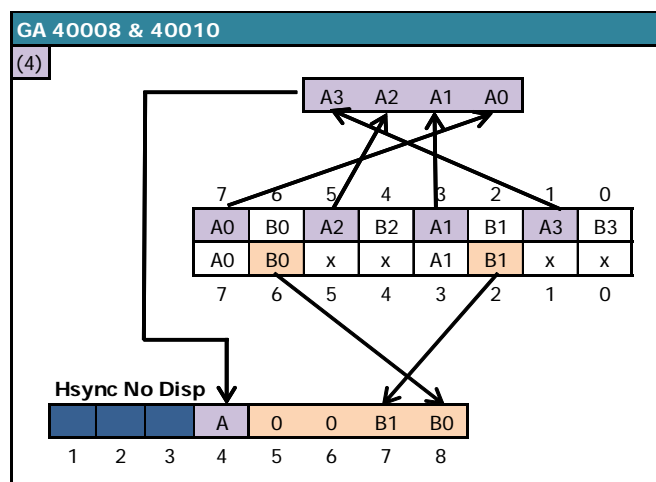
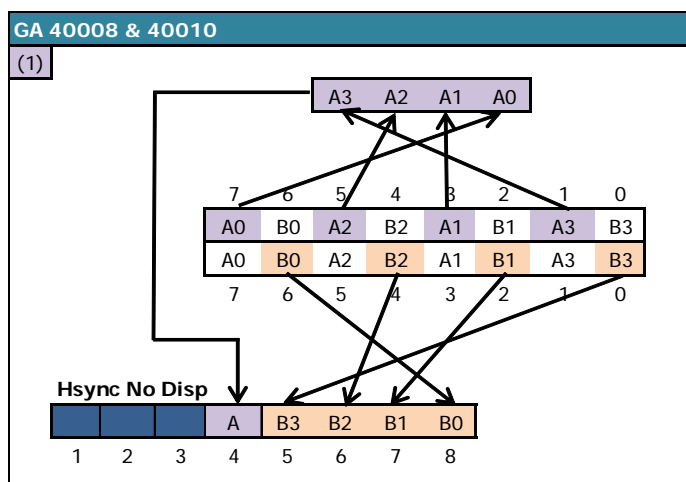
If MODE 2 is the new mode required, then the GATE ARRAY will display 3 new Pixel-M2's after the 4th which represents in total the display of 7 pixels-M2 from the same byte.

If the new required mode is not MODE 2 then the GATE ARRAY will display 4 new Pixel-M2's after the 4th.

Finally, if the new mode required is 1 or 2, then the GATE ARRAY, to calculate the new colour numbers, "reuses" bits already used to calculate the colour number of the previous pixel.

The table below describes the interpretation by the GATE ARRAY 40007, 40008 and 40010 of the VRAM byte processed when the redisplay is activated, according to the new graphic mode requested.

Mode to Mode		VRAM Byte								Displayed Pixels								
0	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp (1)	b0	b4	b2	b6				
0	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp (2)	b2	b6	b1	b5				
0	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp (3)	b6	b5	b4					
0	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp (4)	0	0	b2	b6				
											1	2	3	4	5	6	7	8



When switching from MODE 0 to mode 1 or 2, the common use of the data bits of the byte read in VRAM creates a constraint by linking the colour numbers of the Pixel-M2 displayed in position 4 with that of the pixels located after.

- MODE 0 to MODE 1:** The colour number of the last pixel in MODE 1 corresponds to bits 3 and 4 of the colour number of the 1st pixel in MODE 0.
 - 1st pixel-M2 N° colours 0,1,2,3 = 2nd pixel MODE 1 with colour number 0.
 - 1st pixel-M2 N° colours 4,5,6,7 = 2nd pixel MODE 1 with colour number 1.

- 1st pixel-M2 N° colours 8,9,10,11 = 2nd pixel MODE 1 with colour number 2.
- 1st pixel-M2 N° colours 12,13,14,15 = 2nd pixel MODE 1 with colour number 2.
- **MODE 0 to MODE 2:** The colour number of the 2nd pixel in MODE 2 corresponds to bit 2 of the colour number of the 1st pixel in MODE 0.
 - 1st pixel-M2 No. of colours 0..3, 8..11 = 2nd pixel MODE 2 of colour 0
 - 1st pixel-M2 No. of colours 4..7, 12..15 = 2nd pixel MODE 2 of colour 1

9.3.2.3.3 MODE 1 TO MODE 0.1.2.3

On a line displayed in MODE 1, the data display resumes:

- On CRTC's 0 and 2, from the **4th Pixel-M2 of the 5th VRAM byte.**
- On CRTC 1, from the **5th Pixel-M2 of the 5th VRAM byte.**

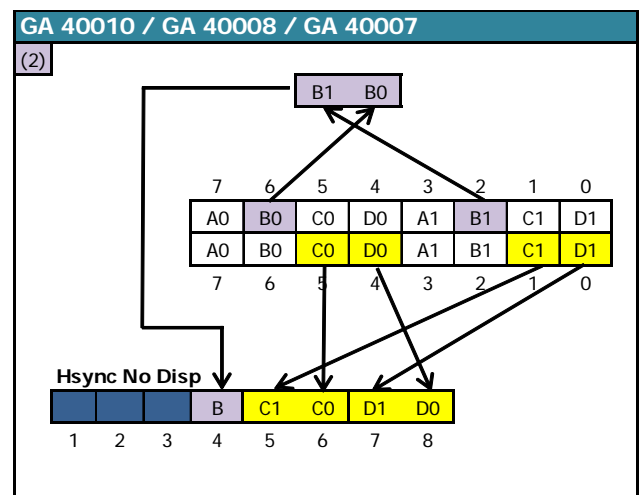
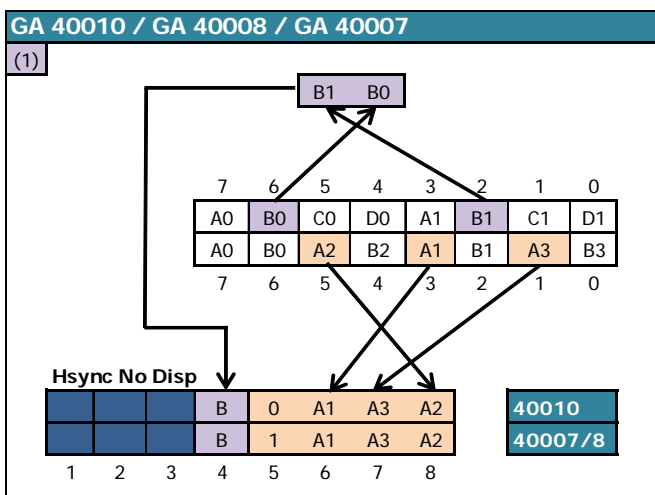
On CRTC's 0 and 2, the first Pixel-M2 displayed is the last of the **2 pixel-M2 of the MODE 1 pixel** displayed in its original colour (i.e. a colour number between 0 and 3). In other words, only half of the MODE 1 pixel is displayed before the GATE ARRAY displays the following pixels.

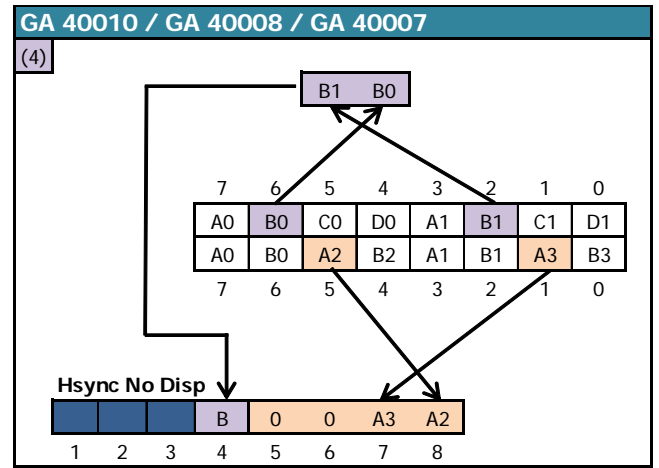
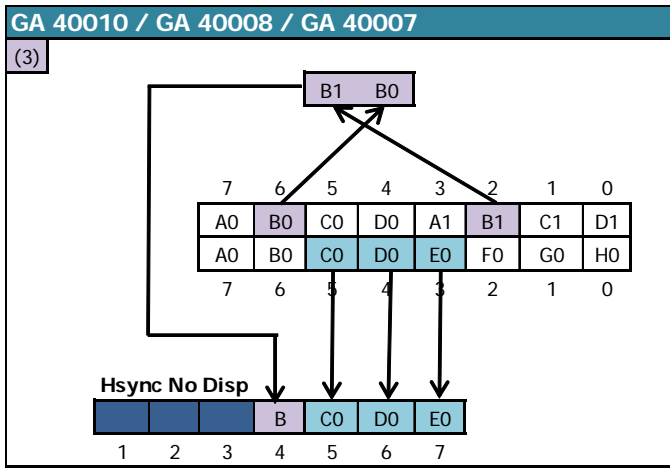
If MODE 2 is the new requested mode, then the GATE ARRAY will display 3 new Pixel-M2's after the 4th, which represents in total the display of 7 pixel-M2's from the same byte.

If the new required mode is different from MODE 2 then the GATE ARRAY will display 4 new Pixel-M2's after the 4th.

The following table describes the interpretation by the GATE ARRAY 40007, 40008 and 40010 of the VRAM byte processed when the display is reactivated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte								Displayed Pixels									
1	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(1)	0/1	b3	b1	b5				
1	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(2)	b1	b5	b0	b4				
1	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(3)	b5	b4	b3					
1	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(4)	0	0	b1	b5				





9.3.2.3.4 MODE 3 TO MODE 0.1.2.3

On a line displayed in MODE 3, the data display resumes:

- On CRTIC's 0 and 2, from the **4th Pixel-M2 of the 5th VRAM byte**.
- On CRTIC 1, from the **5th Pixel-M2 of the 5th VRAM byte**.

On CRTIC's 0 and 2, the first Pixel-M2 displayed is the last of the **4 pixel-M2 of the MODE 3 pixel** displayed in its original colour (i.e. a colour number between 0 and 3). In other words, only ¼ of the MODE 3 pixel is displayed before the GATE ARRAY displays the following pixels.

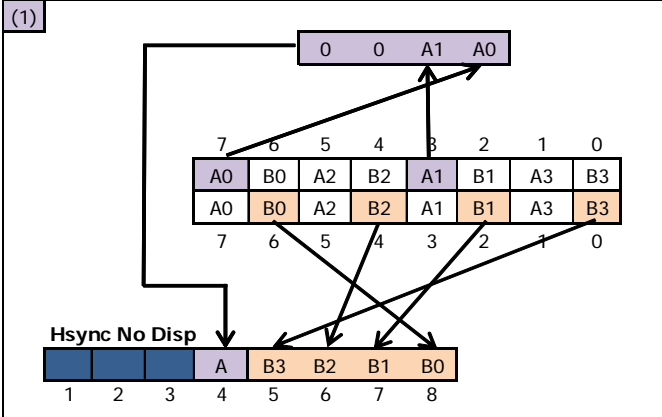
If MODE 2 is the new required then the GATE ARRAY will display 3 new Pixel-M2's after the 4th which represents in total the display of 7 pixel-M2's from the same byte.

If the new required mode is different from MODE 2 then the GATE ARRAY will display 4 new Pixel-M2's after the 4th.

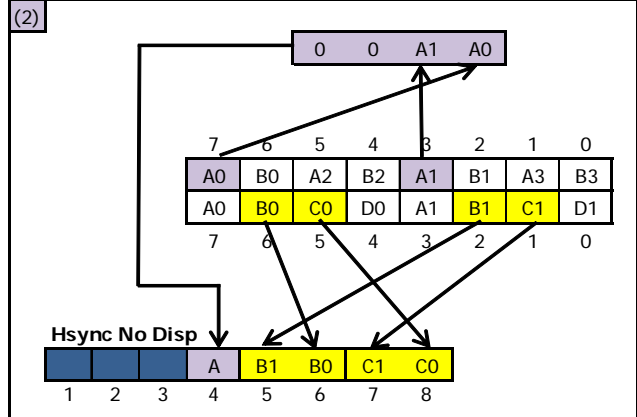
The following table describes the GATE ARRAY's interpretation of the VRAM byte processed when redisplay is enabled, depending on the new graphics mode requested.

Mode to Mode		VRAM Byte								Displayed Pixels									
3	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(1)	b0	b4	b2	b6				
3	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(2)	b2	b6	b1	b5				
3	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(3)	b6	b5	b4					
3	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(4)	0	0	b2	b6				
												1	2	3	4	5	6	7	8

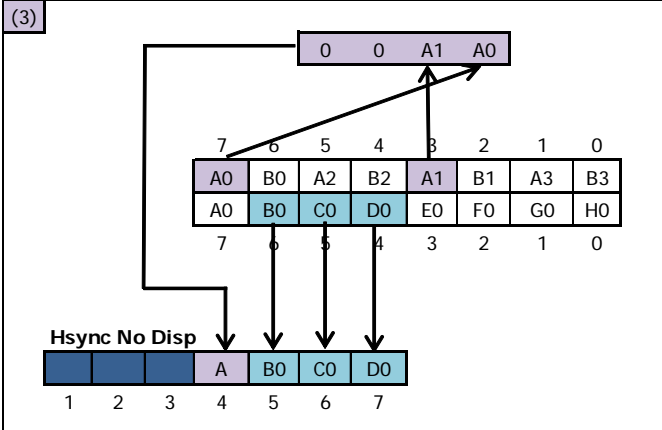
GA 40010 / GA 40008 / GA 40007



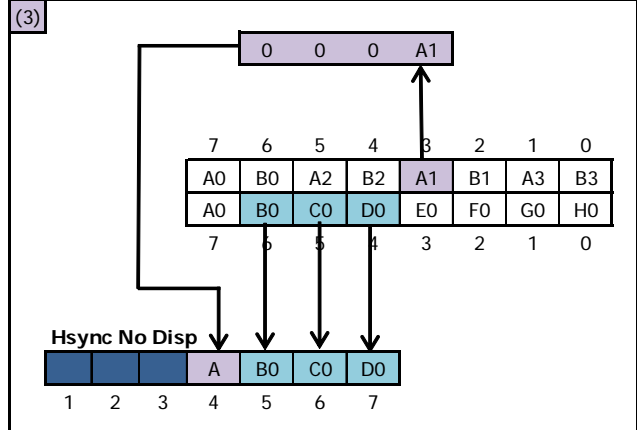
GA 40010 / GA 40008 / GA 40007



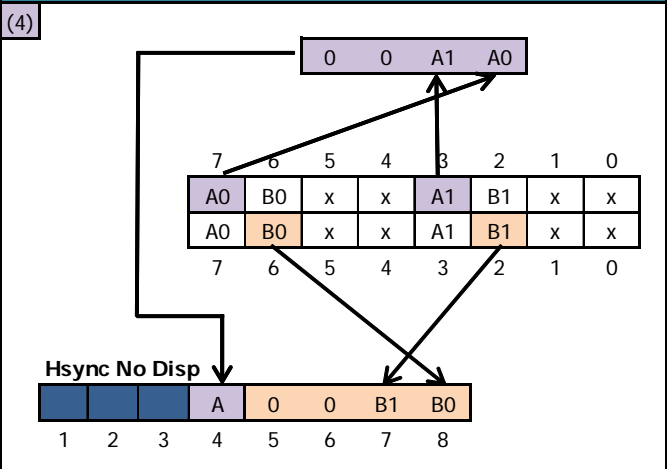
GA 40010



GA 40008 / GA 40007



GA 40010 / GA 40008 / GA 40007



9.3.2.4 CRTIC 0, 1, 2 : PIXEL COOKING WITH R3.JIT

The **R3.JIT** technique can delay the end of an HSYNC by 0.25 μsec.

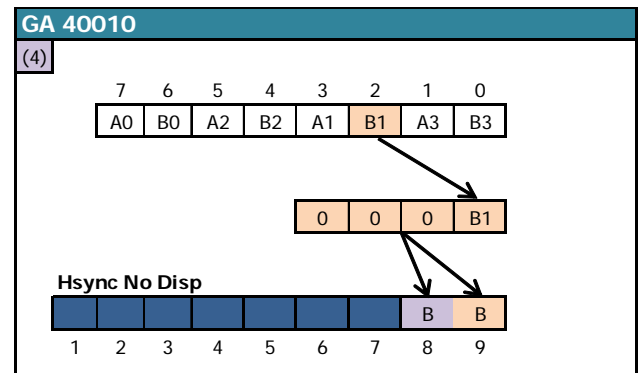
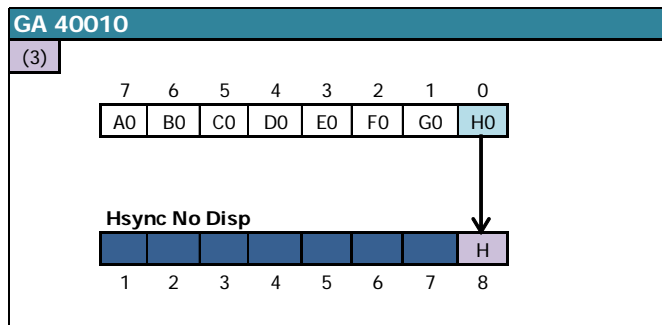
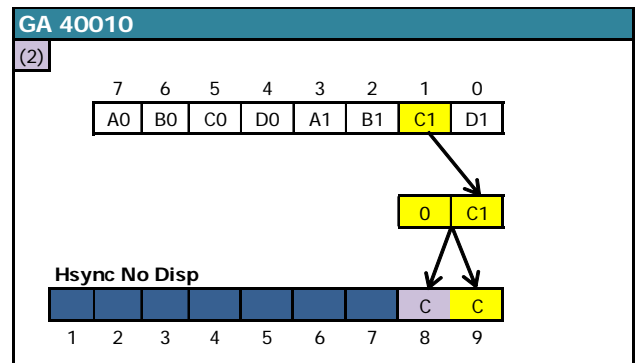
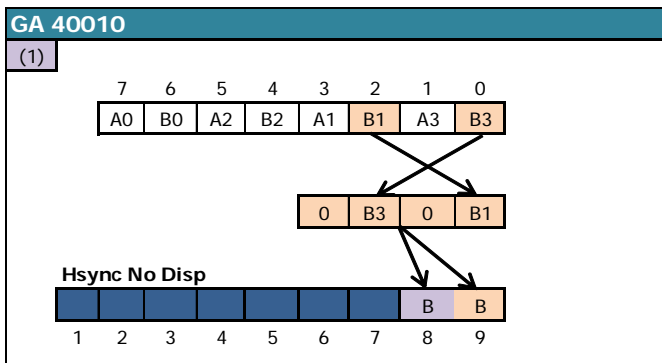
On CRTIC's 0 and 1, the **HSYNC** ceases after the last black Pixel-M2 of the HSYNC.

On CRTIC 2, the **HSYNC** stops on the last Pixel-M2 of the HSYNC and allows the visualization of an additional pixel.

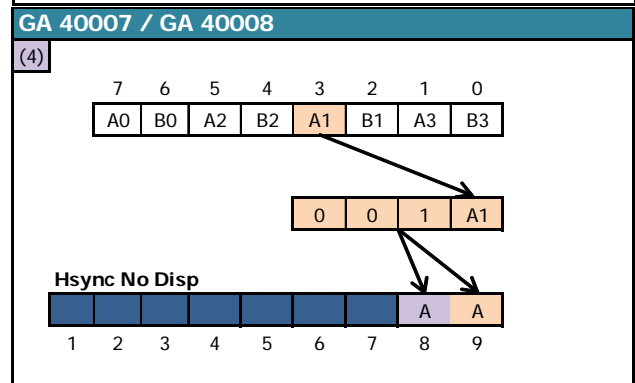
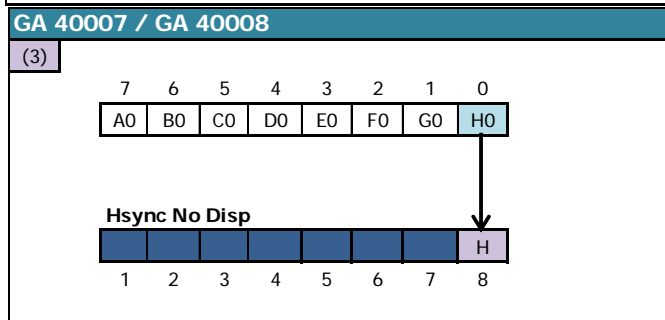
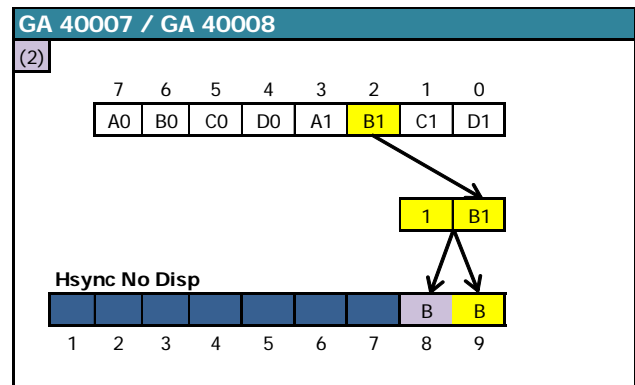
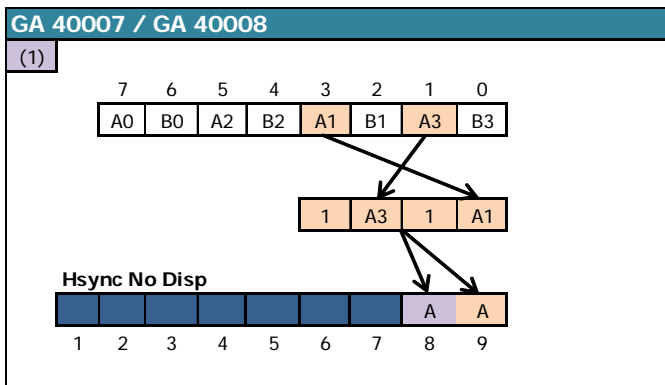
This additional pixel is symbolized in purple on the following diagrams

9.3.2.4.1 MODE 2 TO MODE 0.1.2.3

Mode to Mode	VRAM Byte	GA 40010 : Displayed Pixels																
2	0	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	1	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	2	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	3	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9

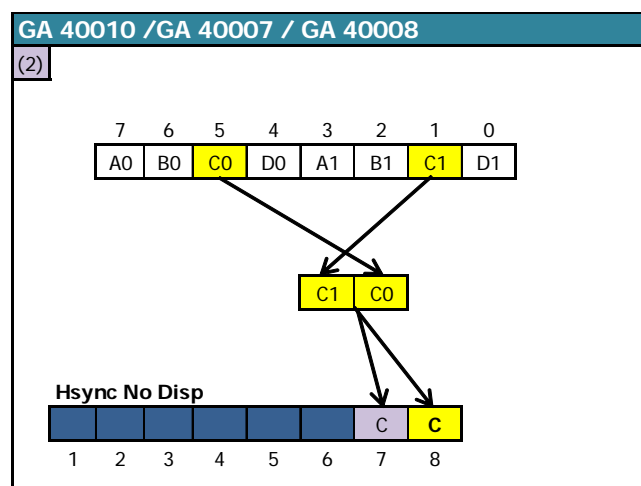
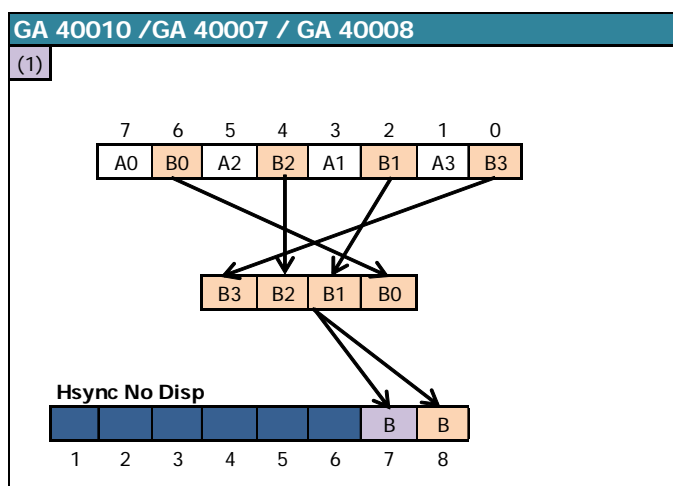


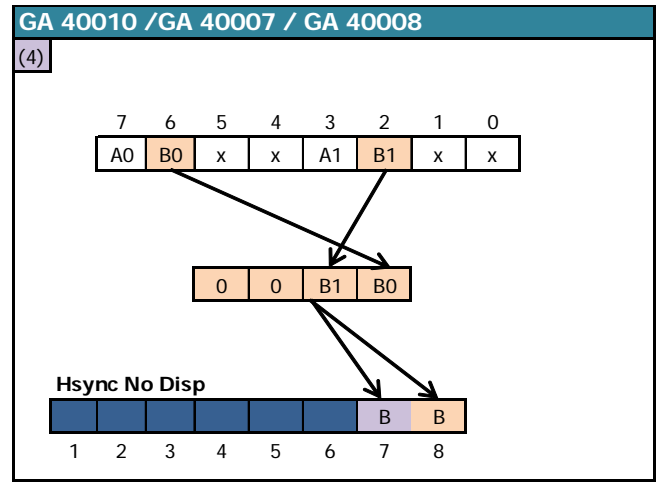
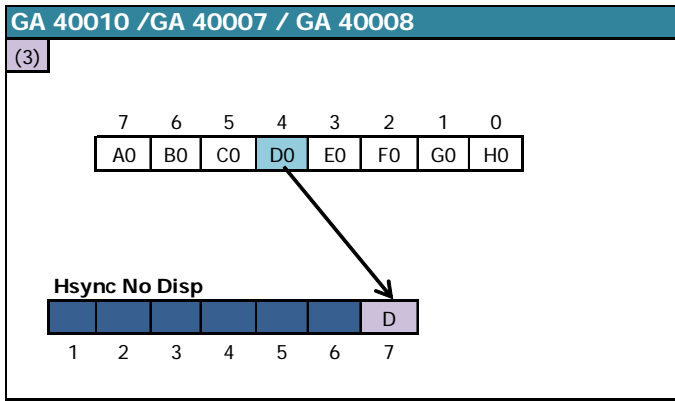
Mode to Mode	VRAM Byte	GA 40007/8 : Displayed Pixels																
2	0	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	1	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	2	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9
2	3	b7	b6	b5	b4	b3	b2	b1	b0	1	2	3	4	5	6	7	8	9



9.3.2.4.2 MODE 0 TO MODE 0.1.2.3

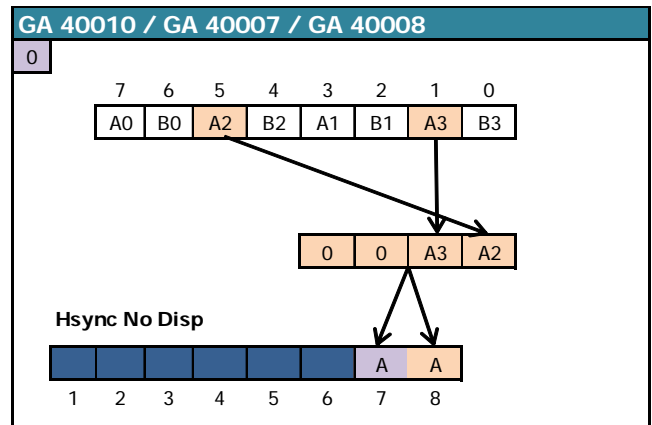
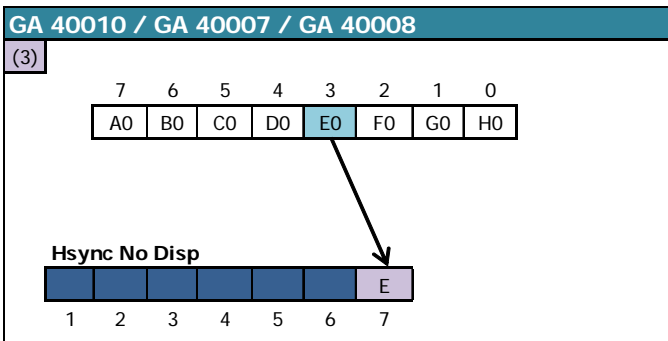
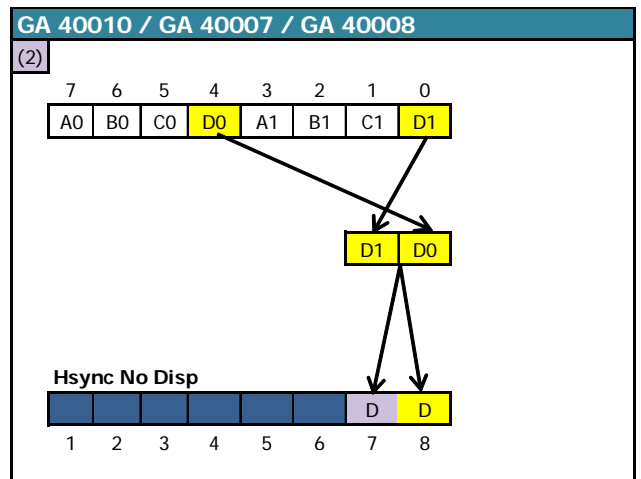
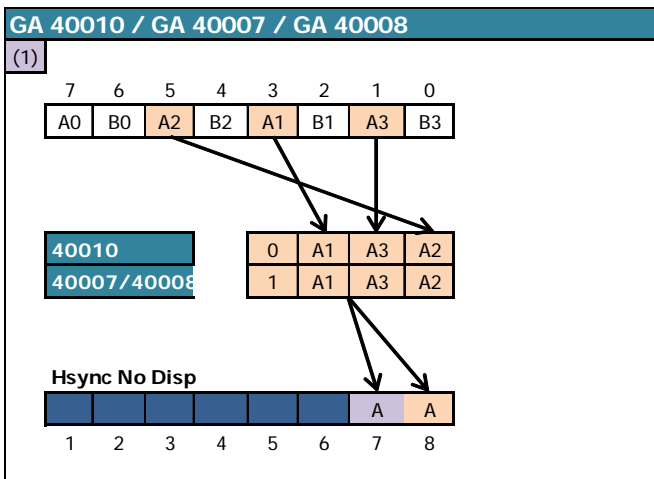
Mode to Mode		VRAM Byte										Displayed Pixels					
0	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp				(1)	(1)		
0	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp				(2)	(2)		
0	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp				(3)			
0	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp				(4)	(4)		
										1	2	3	4	5	6	7	8





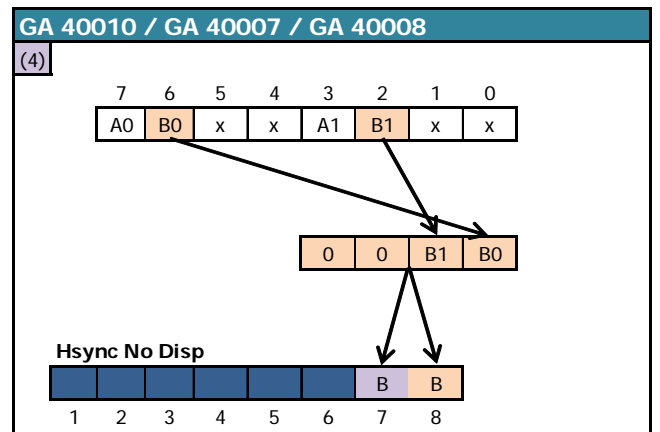
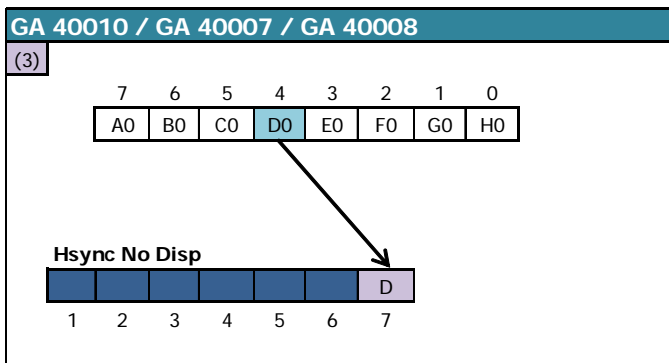
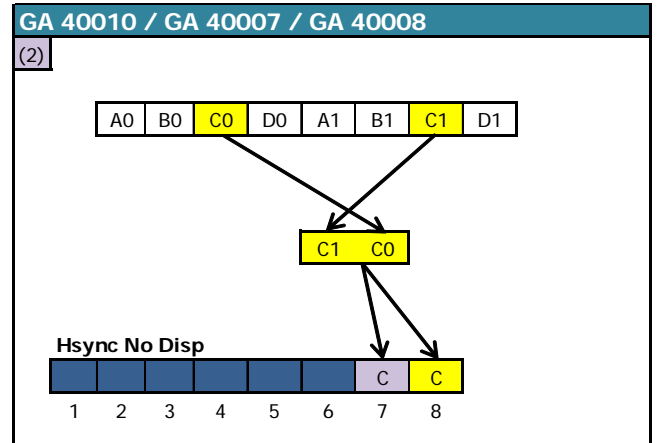
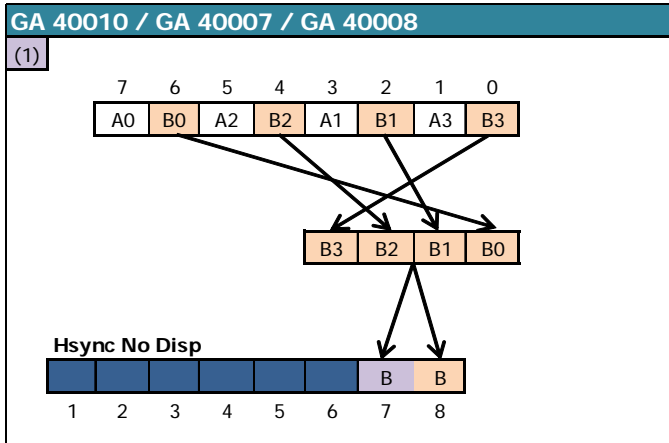
9.3.2.4.3 MODE 1 TO MODE 0.1.2.3

Mode to Mode		VRAM Byte								Displayed Pixels							
1	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(1)	(1)					
1	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(2)	(2)					
1	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(3)						
1	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(4)	(4)					
										1	2	3	4	5	6	7	8



9.3.2.4.4 MODE 3 TO MODE 0.1.2.3

Mode to Mode		VRAM Byte								Displayed Pixels							
3	0	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(1)	(1)					
3	1	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(2)	(2)					
3	2	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(3)						
3	3	b7	b6	b5	b4	b3	b2	b1	b0	Hsync No Disp	(4)	(4)					
										1	2	3	4	5	6	7	8



9.3.2.5 CRTIC 4 : PIXEL COOKING

When the PRE-ASIC switches from one graphics mode to another mode, it is already processing one-byte data according to the previous mode, and the final result obtained reveals its internal logic.

The display stops for 2 μsec (32 Pixel-M2).

The display is restored 1 Pixel-M2 before the PRE-ASIC changes the graphics mode.

The 36th Pixel-M2 displayed therefore has the characteristics of the old mode, for its fraction corresponding to 1 Pixel-M2.

9.3.2.5.1 MODE 2 TO MODE 0.1.2.3

On a line displayed in MODE 2, data display resumes from the **3rd Pixel-M2 of the 7th VRAM byte**.

The first pixel displayed is in MODE 2 (PEN 1 or 0).

Since the MODE 2 pixels are "ahead" of the pixels of the other modes, the PRE-ASIC will display **6 new Pixel-M2's after the 3rd**, unless the mode has not changed.

This represents the display of 9 M2-pixels from a single byte.

The table below describes the interpretation by the PRE-ASIC of the VRAM byte processed when the display is reactivated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte								ASIC 40226: Displayed Pixels									
2	0	b7	b6	b5	b4	b3	b2	b1	b0	No Disp	b5	0.b2.b0.b4		0	b1	0	b3		
2	1	b7	b6	b5	b4	b3	b2	b1	b0	No Disp	b5	b0	b4	0	b3	0	b2		
2	2	b7	b6	b5	b4	b3	b2	b1	b0	No Disp	b5	b4	b3	b2	b1	b0			
2	3	b7	b6	b5	b4	b3	b2	b1	b0	No Disp	b5	0.0.b0.b4		0	0	0	b3		
										1	2	3	4	5	6	7	8	9	

9.3.2.5.2 MODE 0 TO MODE 0.1.2.3

On a line displayed in MODE 0, the data display resumes from **2nd Pixel-M2 of the 7th byte of the VRAM**.

The first Pixel-M2 displayed is the last of the **4 pixel-M2 of the MODE 0 pixel** displayed in its original colour (i.e. a colour number between 0 and 15). In other words, only ¼ of the MODE 0 pixel is displayed before the PRE-ASIC displays the following pixels.

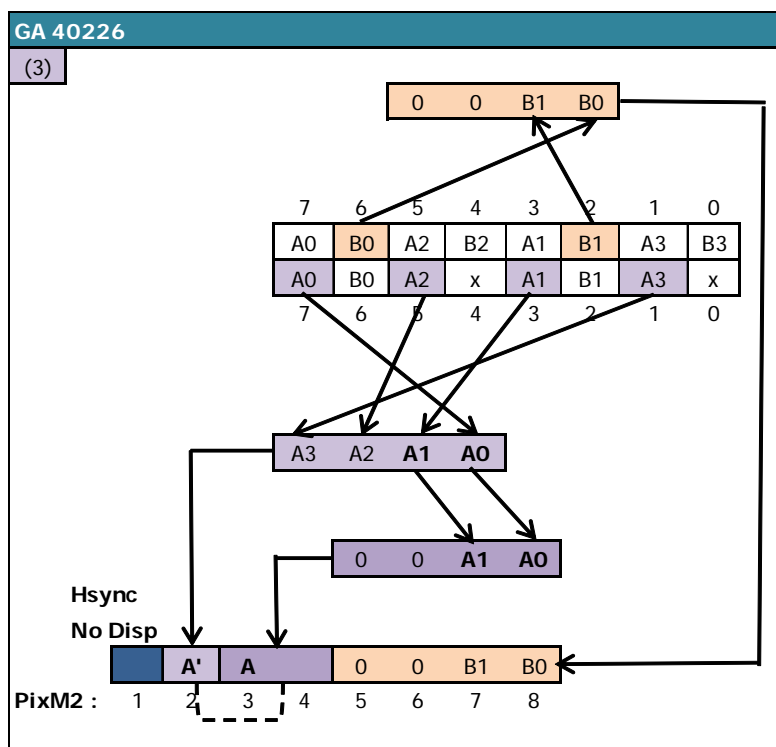
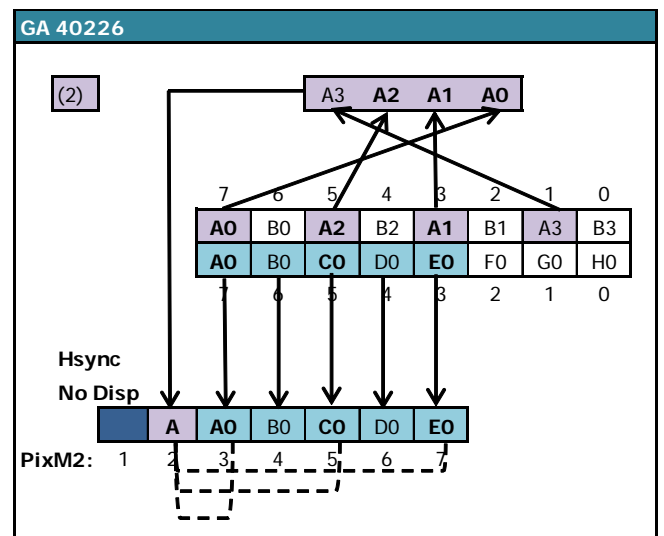
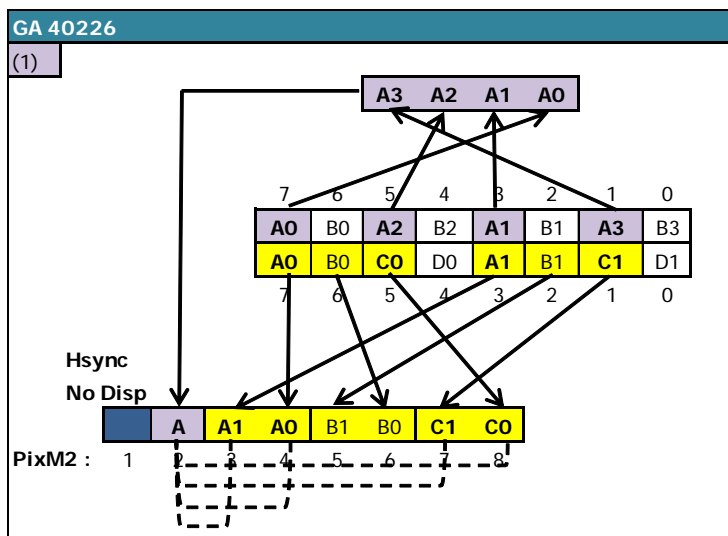
If the new graphics mode required is MODE 2, then the PRE-ASIC displays 5 new Pixel-M2's after the 2nd, which in total represents the display of 7 pixel-M2's from the same byte.

If the new requested mode is different from MODE 2, then the PRE-ASIC displays 6 new Pixel-M2's after the 2nd one.

Finally, if the new required mode is 1 or 2, then the PRE-ASIC, to calculate the new colour numbers, "reuses" bits already used to calculate the colour number of the previous pixel.

The table below describes the interpretation by the PRE-ASIC of the VRAM byte processed when the display is reactivated, according to the new graphics mode requested

Mode to Mode		VRAM Byte								ASIC 40226: Displayed Pixels																																																		
0	0	b7	b6	b5	b4	b3	b2	b1	b0	<table border="1"> <tr> <td></td><td></td><td colspan="4">b1.b5.b3.b7</td><td>b0</td><td>b4</td><td>b2</td><td>b6</td> </tr> <tr> <td>(1)</td><td></td><td>b3</td><td>b7</td><td>b2</td><td>b6</td><td>b1</td><td>b5</td><td></td><td></td> </tr> <tr> <td>(2)</td><td></td><td>b7</td><td>b6</td><td>b5</td><td>b4</td><td>b3</td><td></td><td></td><td></td> </tr> <tr> <td>(3)</td><td>(3)</td><td></td><td></td><td>0</td><td>0</td><td>b2</td><td>b6</td><td></td><td></td> </tr> <tr> <td></td><td></td><td>1</td><td>2</td><td>3</td><td>4</td><td>5</td><td>6</td><td>7</td><td>8</td> </tr> </table>			b1.b5.b3.b7				b0	b4	b2	b6	(1)		b3	b7	b2	b6	b1	b5			(2)		b7	b6	b5	b4	b3				(3)	(3)			0	0	b2	b6					1	2	3	4	5	6	7	8
		b1.b5.b3.b7				b0	b4	b2	b6																																																			
(1)		b3	b7	b2	b6	b1	b5																																																					
(2)		b7	b6	b5	b4	b3																																																						
(3)	(3)			0	0	b2	b6																																																					
		1	2	3	4	5	6	7	8																																																			
0	1	b7	b6	b5	b4	b3	b2	b1	b0																																																			
0	2	b7	b6	b5	b4	b3	b2	b1	b0																																																			
0	3	b7	b6	b5	b4	b3	b2	b1	b0																																																			



9.3.2.5.3 MODE 1 TO MODE 0.1.2.3

On a line displayed in MODE 1, the data display resumes from **2nd Pixel-M2 of the 7th byte of the VRAM**.

The first Pixel-M2 displayed is the last of the **2 pixel-M2 of the MODE 1 pixel** displayed in its original colour (i.e. a colour number between 0 and 3). In other words, only half of the MODE 1 pixel is displayed before the PRE-ASIC displays the following pixels.

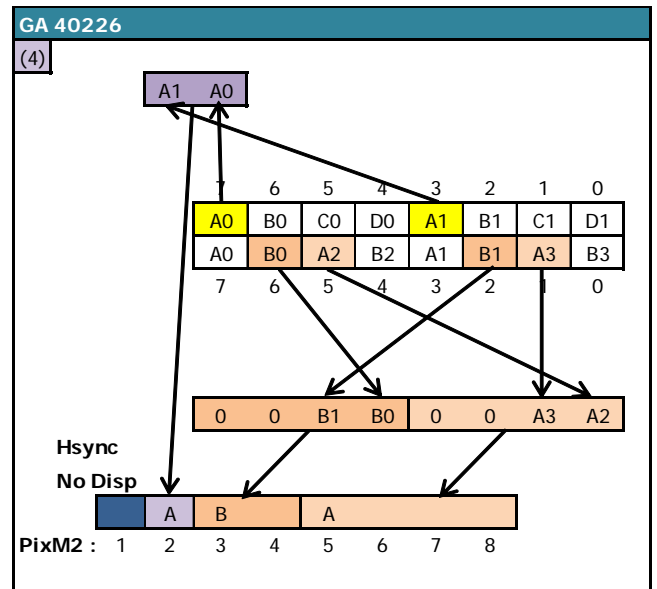
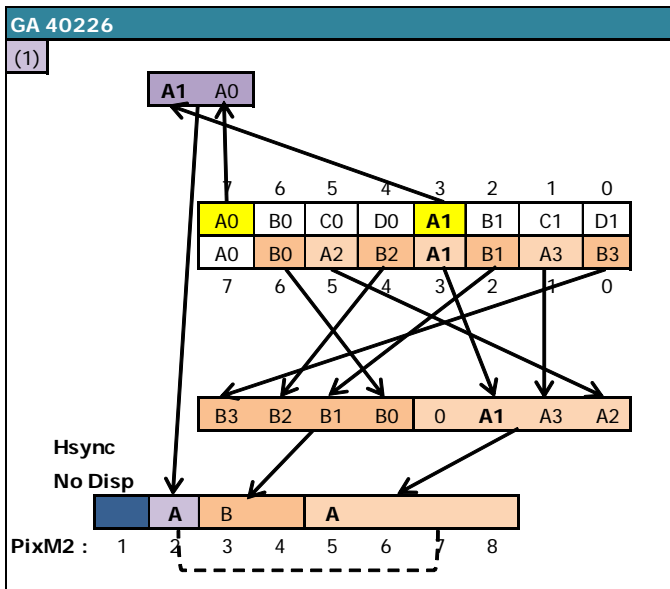
If the new graphics mode required is MODE 2, then the PRE-ASIC displays 5 new Pixel-M2's after the 2nd, which in total represents the display of 7 pixel-M2's from the same byte.

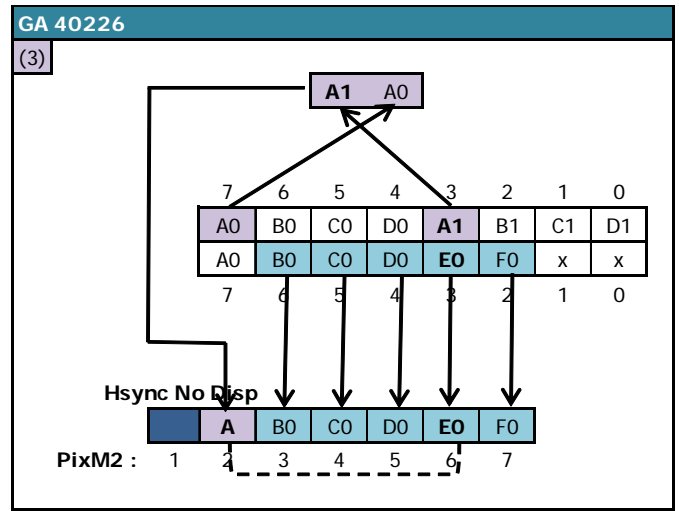
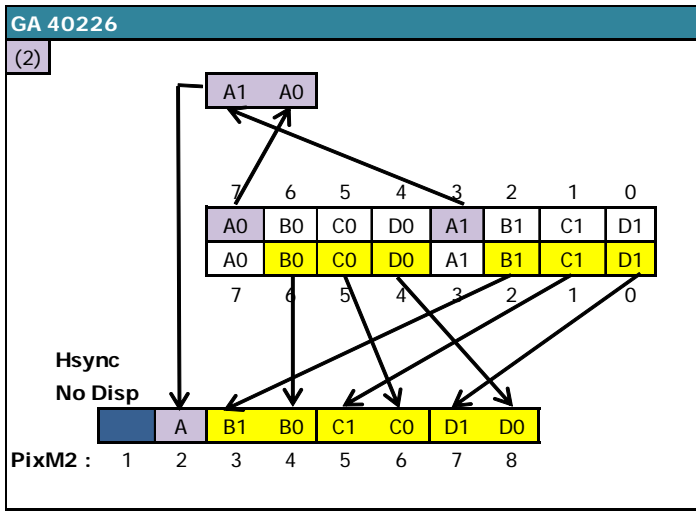
If the new requested mode is different from MODE 2, then the PRE-ASIC displays 6 new Pixel-M2's after the 2nd one.

Finally, if the new mode required is 1 or 2, then the PRE-ASIC, to calculate the new colour numbers, "reuses" bits already used to calculate the colour number of the previous pixel.

The table below describes the interpretation by the PRE-ASIC of the VRAM byte processed when the display is reactivated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte								Displayed Pixels													
1	0	b7	b6	b5	b4	b3	b2	b1	b0	(1)	b0.b4.b2.b6	0	b3	b1	b5								
1	1	b7	b6	b5	b4	b3	b2	b1	b0	(2)	b2	b6	b1	b5	b0	b4							
1	2	b7	b6	b5	b4	b3	b2	b1	b0	(3)	b6	b5	b4	b3	b2								
1	3	b7	b6	b5	b4	b3	b2	b1	b0	(4)	0.0.b2.b6	0	0	b1	b5								
																1	2	3	4	5	6	7	8





9.3.2.5.4 MODE 3 TO MODE 0.1.2.3

On a line displayed in MODE 3, the data display resumes from **2nd Pixel-M2 of the 7th byte of the VRAM**.

The first Pixel-M2 displayed is the last of the **4 pixel-M2 of the MODE 3 pixel** displayed in its original colour (i.e. a colour number between 0 and 3). In other words, only the quarter of the MODE 3 pixel is displayed before the PRE-ASIC displays the following pixels.

If MODE 2 is the new graphics mode required then the PRE-ASIC displays 5 new Pixel-M2's after the 2nd which in total represents the display of 7 pixel-M2's from the same byte.

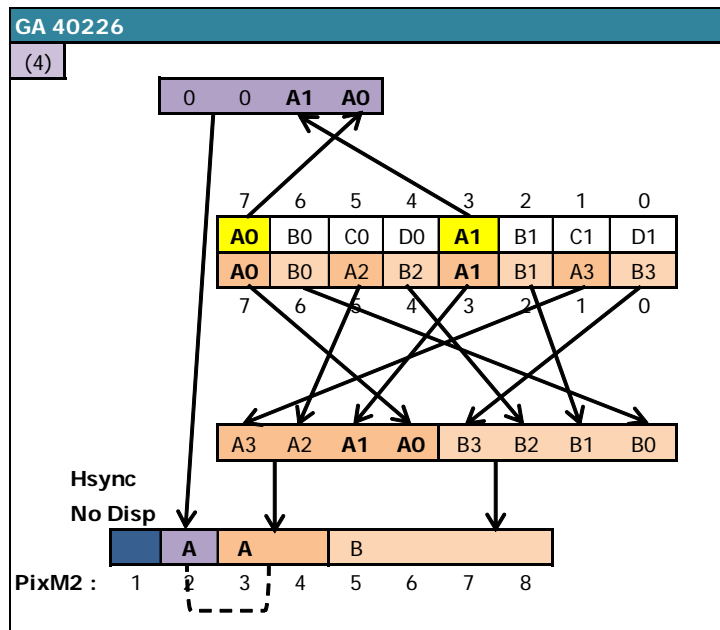
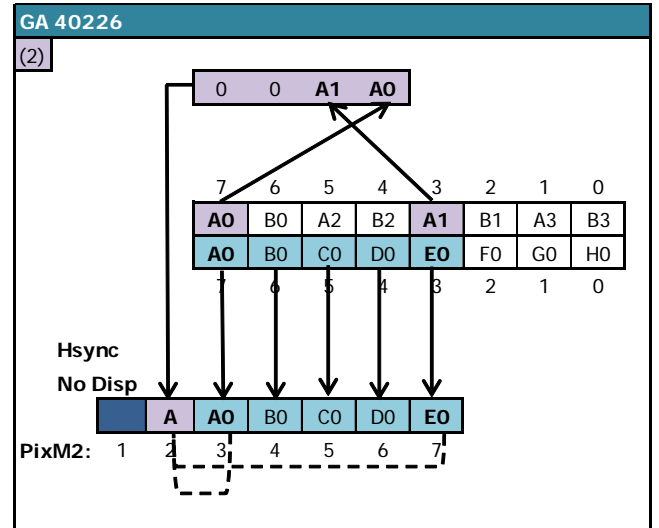
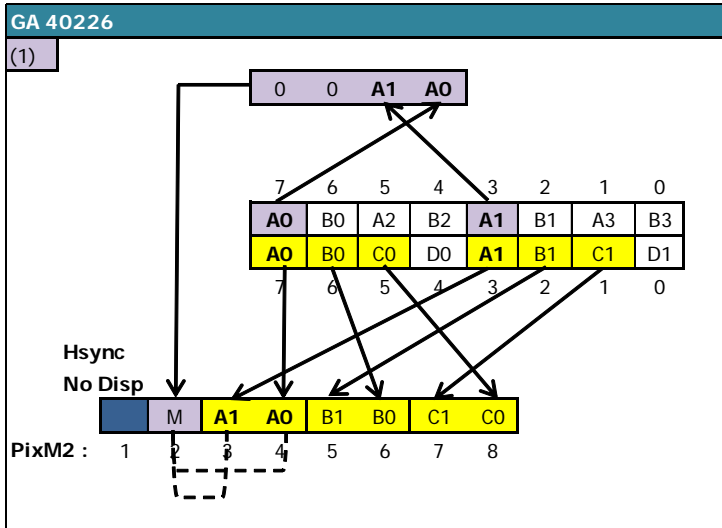
If the new requested mode is different from MODE 2 then the PRE-ASIC displays 6 new Pixel-M2's after the 2nd one.

Finally, if the new mode required is 1 or 2, then the PRE-ASIC, to calculate the new colour numbers, "reuses" bits already used to calculate the colour number of the previous pixel.

The table below describes the interpretation by the PRE-ASIC of the VRAM byte processed when the redisplay is activated, according to the new graphics mode requested.

Mode to Mode		VRAM Byte							
3	0	b7	b6	b5	b4	b3	b2	b1	b0
3	1	b7	b6	b5	b4	b3	b2	b1	b0
3	2	b7	b6	b5	b4	b3	b2	b1	b0
3	3	b7	b6	b5	b4	b3	b2	b1	b0

Displayed Pixels							
	(3)	b1.b5.b3.b7	b0	b4	b2	b6	
	(1)	b3	b7	b2	b6	b1	b5
	(2)	b7	b6	b5	b4	b3	
	0.0.b3.b7	0	0	b2	b6		
1	2	3	4	5	6	7	8



10 COUNTER : REGISTER R9

10.1 GENERAL

Register 9 allows you to set the number of vertical lines of each character line.

In principle, the C9 counter, which determines the raster line of the character line, increments to the value of R9. When IVM interlace mode is enabled, the counting algorithm of C9 is different depending on the CRT type (see Chapter 19.3).

When it returns to 0, C4 is incremented (and in "principle" should return to 0 when C4=R4).

The internal "row" counter C9 is connected directly to the bits 11,12 and 13 of the VRAM pointer. C9 delimits, in a space of 16 KB, 8 slices of 2 KB for 8 different possible "lines".

Extended to 64k of addressable space, this represents 8 slices of 8 KB for the 8 "lines". This principle contributes to the vertical non-linearity of the display ("curtain" effect when the memory is transferred without cutting) well known to any CPC regular.

The definition of R9 is 5 bits which results in "vertical characters" of up to 32 lines. Bits 3 and 4 of the counter are not considered in the calculation of the video pointer on C9 values that exceed 7.

However, this is information that must be considered if C9 is to count beyond 7.

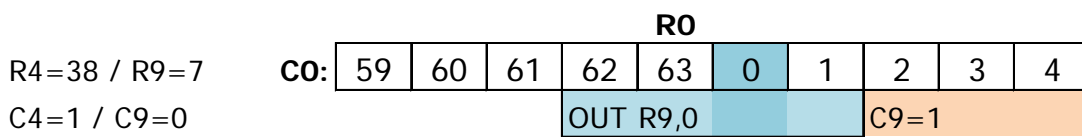
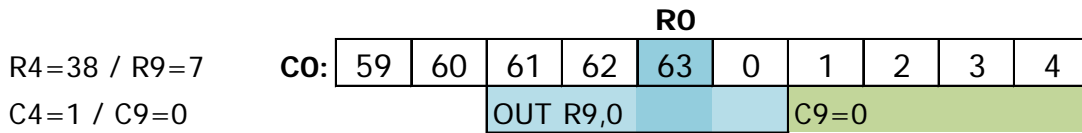
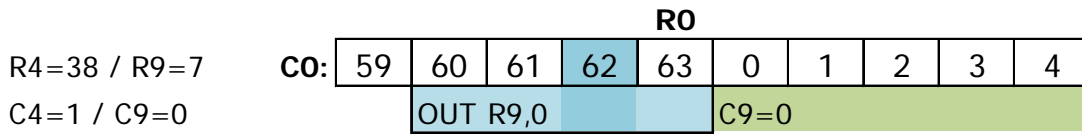
Indeed, even if C9=8 gives the display of a line 0 (bit 3 being "ignored"), this value does not always allow for the consideration of the operations that take place during the change of a line-character (C4).

10.2 TIME LIMITS

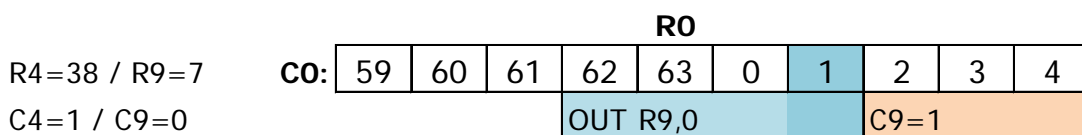
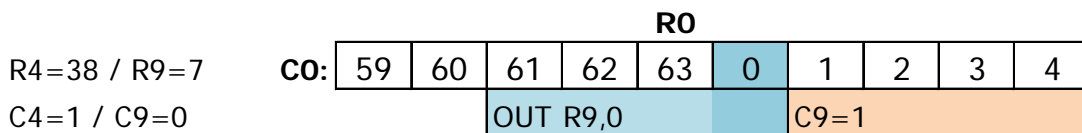
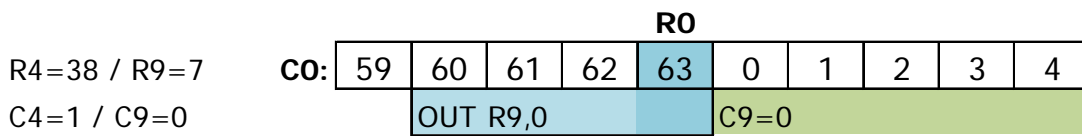
R9 update is considered while $C0 \leq R0$.

In the diagrams below, R9 is set to 0 when it was greater than 0 before.

CRTC 0, 1, 2



CRTC 3, 4



10.3 COUNTING RULES

If R9 is updated with 0 while C9 is greater than 0, for example, C9 will count to its maximum value (31) before going back to 0.

There is an exception to this rule for CRTC's 0 and 2, when R9 is updated with 0 on the last line of the last character of the screen.

10.3.1 CRTIC 0

It can be read quite often that the modification of R9 on CRTIC 0 (and 2) is not considered for the line that follows the one where the update took place because the counter for this register would be "buffered". The only value that is saved in a buffer in the CRTIC is the video pointer because it is discarded at each line start. (see Chapters 17 and 20.2).

However, the CRTIC does not "buffer" its counters. **It simply tests the equivalence of the counters with its registers at very precise moments.** In this case, the value of C9 is compared with R9 when C0=0 (as well as C4 with R4) to determine if the line was the last on the screen.

This comparison takes place only to decide whether C4 will be reset to 0 or whether C4 will be incremented.

Indeed, C4 is a counter that must "**officially**" be able to exceed R4, especially in vertical adjustment.

Note : CRTIC's 3 and 4, for which C4 does not exceed R4 in adjustment, "solidifies" the additional lines with C4=R4.

If R9 or R4 are modified after C0 has exceeded 0, it does not change anything. Case closed. When C4 is incremented, C9 necessarily goes to 0 (except when R0=0).

Apart from this particular processing management of C4 on the last line of a screen, **the update of R9 is considered immediately.**

10.3.1.1 GENERAL CASE

If R9 is changed with the value of C9, it will change to 0 on the next line.

Example : C9=0 and R9 is updated with 0, which was 7 before.

Example : C9=3 and R9 is updated with 3, which was 7 before.

If R9 is modified with a value less than C9, then C9=C9+1 (overflow of C9)

Example : C9=3 and R9 is updated with 1. Next C9 will be 4.

If the C9 counter overflows, it will count to its maximum value (31) before looping back to 0.

If R9 is modified with a value greater than C9, then C9=C9+1. C4 is unchanged.

Example : C9=0 and R9 is updated with 7. C9 will be 1 on the next line.

10.3.1.2 EXCEPTION TO THE GENERAL CASE : LAST LINE OF SCREEN

Updating R9 on this last line when C0>1 has no impact on the next C9, because C4 will be forced to 0 and therefore C9 will also change to 0.

If C4=R4 and C9=R9 when C0=0, then the "**last screen line**" state is lifted. In this situation, C4 will be reset to 0 (excluding additional lines), and C9 will change to 0 regardless of the value programmed in R9 afterwards.

If C4=R4 and C9<>R9 when C0=0, then C4 will be incremented no matter what. In this situation, if R9 is changed on this line with the value of C9, then C9 will change to 0 but C4 will be incremented by 1.

The "last line" status is tested at the very beginning of the C0=0 management.

- If an R9 update occurs when C0=0, then the last line state will not be lifted.
- If an update of R9 takes place when C0=1, then the additional management takes place and R5 replaces R9 (C9+1=R5)

10.3.2 CRTC 1

10.3.2.1 GENERAL CASE

If R9 is changed to the current value of C9, then on the following line:

C9 goes to 0.

C4 is incremented by 1, and goes to 0 if it was R4, and in this case the offset is considered.

If R9 is modified with a value less than C9

C9=C9+1 and C4 is unchanged (until the end of the overflow of C9).

The offset will be changed only if C4=C9=C0=0

If R9 is modified with a value greater than C9, then C9=C9+1. C4 is unchanged.

Example : C9=0 and R9 is updated with 7. C9 will be 1 on the next line.

10.3.2.2 NO EXCEPTION

Everything is pure logic, in an unspeakable and tasteless simplicity. :-)

10.3.3 CRTC 2

10.3.3.1 GENERAL CASE

If R9 is changed with the value of C9, it will change to 0 on the next line.

Example : C9=0 and R9 is set to 0, which was 7 before.

Example : C9=3 and R9 is set to 3, which was 7 before.

If R9 is modified with a value less than C9, then C9=C9+1 (overflow of C9).

Example : C9=3 and R9 is set to 1. C9 will be 4.

If the C9 register overflows, it will count to its maximum value (31) before looping back to 0.

If R9 is modified with a value greater than C9, then C9=C9+1. (C4 is unchanged).

Example : C9=0 and R9 is set to 7. C9 will be equal to 1 on the next line.

10.3.3.2 EXCEPTIONS TO THE GENERAL CASE

When C4=R4 and C9=R9 **during the first HSYNC**, a "last screen line" state is lifted, which can no longer be cancelled. If R9 is updated to C0=0 when C4=R4 and C9=R9, then the last line state is not enabled.

Updating R9 in this situation has no impact on the next C9, as **C4 will be forced to 0** and C9 will also be zeroed.

When the reset of C4 to 0 is armed, it is no longer possible to cancel it, unless the last line condition is still true **with the same C9/R9 during the second HSYNC. In this case, the reset to 0 of C4 is irrevocably cancelled.**

If C9 is equal to R9, then C4 will be incremented regardless of the value of R4 (even if C4=R4).

If R9 has been modified (C9<>R9) then C9 will increment (C4 will not be modified).

If the objective is to maintain the reset of C4 to 0, it is possible to prevent the arming of the irrevocable increment of C4/C9 described above by changing the last line condition for the values of C0 during which HSYNC takes place.
See RLAL/RVLL Chapter 12.4.1, page 87.

10.3.4 CRTC 3, 4

10.3.4.1 GENERAL CASE

When R9 is changed, its value is considered immediately in the following way.

If R9 is changed with a value less than or equal to C9, then C9 changes to 0 on the next line, and C4 goes to 0 (if C4=R4) otherwise C4=C4+1.

Simply put, it is impossible to "overflow" C9 on these CRTC's.

It is not a simple equality test which takes place, but a "more complex" comparison performed by the ASIC:

If current-C9 > R9 then next-C9=0

Example : If C9 was 4, and R9 is changed with 1 (whereas it was 7 before), then C9 will go to 0 (and C4=C4+1 or 0 depending on the value of C4 and R4)

After C9=0, C9 will be incremented to the new value of R9. 1 in the example.

This management sometimes allows for dual compatibility with CRTC's 0, 1 and 2.

Indeed, if a program modifies R9 as part of a line-to-line rupture, a classic way to proceed is to:

- Update R9=0 on the last line of the screen on CRTC 0 or 2, so that the next line C9=0 is also considered the last screen (if R4=0).
- Update R9=0 on the first line of the screen on CRTC 1, so that the next line is considered the last screen (if R4=0).

In both situations, CRTC's 3 and 4 will put C9=0 back on the next line.

Previous R9=7 C4=R4				CRTC 0 (HD6845SP) Result on next line			CRTC 1 (UM6845R) Result on next line			CRTC 2 (MC6845P) Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	7	0	0	0	C4=C4+1 (*)	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
2	7	1	0	C9=C9+1 (2)	unmodified	No	C9=C9+1 (2)	unmodified	Yes if C4=0	C9=C9+1 (2)	unmodified	No	0	0	Yes
3	7	2	0	C9=C9+1 (3)	unmodified	No	C9=C9+1 (3)	unmodified	Yes if C4=0	C9=C9+1 (3)	unmodified	No	0	0	Yes
4	7	3	0	C9=C9+1 (4)	unmodified	No	C9=C9+1 (4)	unmodified	Yes if C4=0	C9=C9+1 (4)	unmodified	No	0	0	Yes
5	7	4	0	C9=C9+1 (5)	unmodified	No	C9=C9+1 (5)	unmodified	Yes if C4=0	C9=C9+1 (5)	unmodified	No	0	0	Yes
6	7	5	0	C9=C9+1 (6)	unmodified	No	C9=C9+1 (6)	unmodified	Yes if C4=0	C9=C9+1 (6)	unmodified	No	0	0	Yes
7	7	6	0	C9=C9+1 (7)	unmodified	No	C9=C9+1 (7)	unmodified	Yes if C4=0	C9=C9+1 (7)	unmodified	No	0	0	Yes
8	7	7	0	0	0	Yes	C9=C9+1 (8)	unmodified	Yes if C4=0	0	0	If C0<=R1	0	0	Yes

(*) overflow

Previous R9=7 C4<>R4				CRTC 0 (HD) Result on next line			CRTC 1 Result on next line			CRTC 2 Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	7	0	0	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
2	7	1	0	C9=C9+1 (2)	unmodified	No	C9=C9+1 (2)	unmodified	Yes if C4=0	C9=C9+1 (2)	unmodified	No	0	C4=C4+1	No
3	7	2	0	C9=C9+1 (3)	unmodified	No	C9=C9+1 (3)	unmodified	Yes if C4=0	C9=C9+1 (3)	unmodified	No	0	C4=C4+1	No
4	7	3	0	C9=C9+1 (4)	unmodified	No	C9=C9+1 (4)	unmodified	Yes if C4=0	C9=C9+1 (4)	unmodified	No	0	C4=C4+1	No
5	7	4	0	C9=C9+1 (5)	unmodified	No	C9=C9+1 (5)	unmodified	Yes if C4=0	C9=C9+1 (5)	unmodified	No	0	C4=C4+1	No
6	7	5	0	C9=C9+1 (6)	unmodified	No	C9=C9+1 (6)	unmodified	Yes if C4=0	C9=C9+1 (6)	unmodified	No	0	C4=C4+1	No
7	7	6	0	C9=C9+1 (7)	unmodified	No	C9=C9+1 (7)	unmodified	Yes if C4=0	C9=C9+1 (7)	unmodified	No	0	C4=C4+1	No
8	7	7	0	C9=C9+1 (8)	unmodified	No	C9=C9+1 (8)	unmodified	Yes if C4=0	C9=C9+1 (8)	unmodified	No	0	C4=C4+1	No

Previous R9=7 C4=R4				CRTC 0 (HD) Result on next line			CRTC 1 Result on next line			CRTC 2 Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	7	0	0	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
2	7	1	1	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
3	7	2	2	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
4	7	3	3	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
5	7	4	4	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
6	7	5	5	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
7	7	6	6	0	C4=C4+1	No	0	0	Yes	0	0	If C0<=R1	0	0	Yes
8	7	7	7	0	0	Yes	0	0	Yes	0	0	If C0<=R1	0	0	Yes

Previous R9=7 C4<>R4				CRTC 0 (HD) Result on next line			CRTC 1 Result on next line			CRTC 2 Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	7	0	0	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
2	7	1	1	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
3	7	2	2	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
4	7	3	3	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
5	7	4	4	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
6	7	5	5	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
7	7	6	6	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No
8	7	7	7	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No	0	C4=C4+1	No

Previous R9=7 C4=R4				CRTC 0 (HD) Result on next line			CRTC 1 Result on next line			CRTC 2 Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	7	0	2	C9=C9+1 (1)	unmodified	No	C9=C9+1 (1)	unmodified	Yes if C4=0	C9=C9+1 (1)	unmodified	No	0	0	Yes

Previous R9=0 C4=R4=0				CRTC 0 (HD) Result on next line			CRTC 1 Result on next line			CRTC 2 Result on next line			CRTC 3, 4 Result on next line		
Case	R9	C9 cur	Upd R9	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd	C9	C4	Offs Upd
1	0	0	0	0	0	Yes	0	0	Yes	0 (*)	C4=0 / C4+1	Yes (C0<=R1)	0	0	Yes
2	0	0	1	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
3	0	0	2	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
4	0	0	3	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
5	0	0	4	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
6	0	0	5	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
7	0	0	6	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No
8	0	0	7	0	0	Yes	C9=C9+1 (1)	0	Yes (C4=0)	0 / 1 (*)	C4=0 / C4+1	Yes (C0<=R1)	C9=C9+1 (1)	0	No

(*) According cancelation of C4 zeroed in Hsync - See chapter

11 COUNTER : REGISTER R5

11.1 GENERAL

The R5 register allows you to add so-called vertical adjustment lines at the end of the screen. The objective of this register is to complete the total number of rows displayed when $(R4+1) \times (R9+1)$ applied during a frame does not correspond to 312 rows (for the European standard)

This register contains a number of lines on 5 bits (0 to 31) which corresponds to the maximum possible adjustment compared to the maximum number of possible lines of a character, fixed by R9. Indeed, even if CRTC's 1, 2, 3 and 4 do not respect this functional principle, the adjustment is not supposed to contain several characters. In other words, if $R5/R9+1 > 1$, R4 should be adjusted.

When $C4=R4$, $C9=R9$ and $C0=R0$, then $C5=0$ and $C9=0$.

If $R5 = 0$ then there is no specific adjustment.

If $R5 < > 0$ then an adjustment takes place with the creation of additional lines.

However, if one of the two interlace modes is programmed ($R8=1$ or $R8=3$) then an additional line is added on the even screens, as if $C5$ were equal to -1.

The implementation of the vertical adjustment function is the source of several differences between the CRTC's, with generally positive consequences. During this creation of complementary lines, the $C5$ and $C9$ counters are incremented, and sometimes $C4$:

- On CRTC 0, $C4$ is incremented only once since $C5$ does not exist, and it is $C9$ which is compared to $R5$ and $R9$.
- On CRTC's 1 and 2, $C4$ increments regardless of the value of $R4$ each time $C9=R9$.
- On CRTC's 3 and 4, $C4$ does not increment.

$R1$ management for updating the video pointer continues to be provided during this management of additional lines on CRTC's 0, 1 and 2 when $C9=R9$.

$C4$ is then reset to 0.

$R7$ can be positioned on one of the values reached by $C4$ in vertical adjustment to trigger a VSYNC.

$R6$ must be positioned according to the values reached by $C4$ to display the corresponding characters.

11.2 COUNTING IN VERTICAL ADJUSTEMENT

11.2.1 GENERAL

The following diagrams describe the diversity of the methods of counting (C4, C9, C5) and updating the video pointer during this management, considering that R5 and R9 are not modified during the adjustment. The registers are initialized as follows (R4=10, R5=16, **R9=3**, R1=40, R0=63)

CRTC 0			
C4	C9	C5	PTR-VRAM LINE
11	0	0	0 &0
11	1	1	0 &800
11	2	2	0 &1000
11	3	3	0 &1800
11	4	4	40 &2000
11	5	5	40 &2800
11	6	6	40 &3000
11	7	7	40 &3800
11	8	8	40 &0
11	9	9	40 &800
11	10	10	40 &1000
11	11	11	40 &1800
11	12	12	40 &2000
11	13	13	40 &2800
11	14	14	40 &3000
11	15	15	40 &3800

CRTC 1, 2			
C4	C9	C5	PTR-VRAM LINE
11	0	0	0 &0
11	1	1	0 &800
11	2	2	0 &1000
11	3	3	0 &1800
12	0	4	40 &0
12	1	5	40 &800
12	2	6	40 &1000
12	3	7	40 &1800
13	0	8	80 &0
13	1	9	80 &800
13	2	10	80 &1000
13	3	11	80 &1800
14	0	12	120 &0
14	1	13	120 &800
14	2	14	120 &1000
14	3	15	120 &1800

CRTC 3, 4			
C4	C9	C5	PTR-VRAM LINE
10	0	0	0 &0
10	1	1	0 &800
10	2	2	0 &1000
10	3	3	0 &1800
10	0	4	0 &2000
10	1	5	0 &2800
10	2	6	0 &3000
10	3	7	0 &3800
10	0	8	0 &0
10	1	9	0 &800
10	2	10	0 &1000
10	3	11	0 &1800
10	0	12	0 &2000
10	1	13	0 &2800
10	2	14	0 &3000
10	3	15	0 &3800

11.2.2 CRTC 0

On CRTC 0, HITACHI engineers saved a C5 counter to use C9 instead. The new limit of C9 is no longer R9 but R5-1 (R5 must be greater than 0 for there to be at least one line generated, except in the context of interlace modes).

The additional management then simply inhibits the reset of C9 to 0.

It is not "convenient" to manage several characters automatically during the adjustment, but it allows you to switch to another address without C9 being equal to 0.

Indeed, **the C9=R9 management continues to consider the video pointer (VMA'=VMA) when C0=R1.**

Thus, the diagram on the next page, which uses the data from the first diagram shows the impact of an R9 update being adjusted to change the VMA' pointer.

CRTC 0				
C4	C9	C5	PTR-VRAM	LINE
11	0	0	0	&0
11	1	1	0	&800
11	2	2	0	&1000
11	3	3	0	&1800
11	4	4	40	&2000
11	5	5	40	&2800
11	6	6	40	&3000
11	7	7	40	&3800
11	8	8	40	&0
11	9	9	40	&800
11	10	10	40	&1000
11	11	11	80	&1800
11	12	12	80	&2000
11	13	13	80	&2800
11	14	14	80	&3000
11	15	15	80	&3800

R9

OUT R9,10

R9

11.2.3 CRTC 1, 2

On these circuits, the C5 and C9 counters are dissociated.

The C9=R9 management considers the video pointer (VMA'=VMA) and increments C4 when C0=R1, but resets C9 to 0 when C9=R9.

R9 update is considered for current C9 counting.

CRTC 1, 2				
C4	C9	C5	PTR-VRAM	LINE
11	0	0	0	&0
11	1	1	0	&800
11	2	2	0	&1000
11	3	3	0	&1800
12	0	4	40	&0
12	1	5	40	&800
12	2	6	40	&1000
12	3	7	40	&1800
12	4	8	40	&2000
12	5	9	40	&2800
12	6	10	40	&3000
12	7	11	40	&3800
12	8	12	40	&0
12	9	13	40	&800
12	10	14	40	&1000
13	0	15	80	&0

R9

OUT R9,10

R9

11.2.4 CRTC 3, 4

On CRTC's 3 and 4, the C4 counter is not incremented.

This "solidifies" the last character with the character generated in vertical adjustment.

In the previous example, the character C4=10 contains 16 more rows.

The 10th,11th and 12th bits of the pointer come from bits 0,1 and 2 of C5 (not C9).

11.3 UPDATING R5 DURING AN ADJUSTMENT

If R5 is changed with C5+1 on the current line, then the vertical adjustment is "stopped".

In this situation, C4=C9=0 for the next line (regardless of the current value of C9).

The "last line" state is then true and leads to the reset of C4 to 0.

However, if R5 is changed (slyly?) to 0, then C4 is not reset to 0 and this causes C4 overflow.

The vertical adjustment algorithm is then disabled, and C4 counts up to its maximum value to loop back.

In general, except in special cases, R4 has been exceeded and C4 then counts up to its maximum value to loop back to R4.

11.4 CRTC 0 : UNSOLICITED ADJUSTMENT

On CRTC 0, disabling C9=R9 management in adjustment suggests that C5 does not exist on this circuit. Thus, as indicated in the chapter dedicated to the R0 register, if C0 does not reach 2 on a last line of screen, then the additional management is activated. Since CRTC 0 was the first CRTC created, we can assume that the engineers sought to save counter.

Only one line is displayed because if C9 goes back to 0, it reaches R5=0.

On the other hand, if C9 has incremented (case of overflow documented in Chapter 13.6.2.2) then the additional management continues while $C9+1 < > R5$.

11.5 RUPTURE FOR DUMMIES (R.F.D.) ON CRTC 1

On the CRTC 1, there is a very interesting bug when R5 is updated with a value different from 0 on the position $C0=R0$ of some C9s when R5 is equal to 0.

I name **RFD** the rupture technique that stems from this bug.

Activating an **RFD** sets several statuses.

- The first status defines the VMA update source (VMA' or R12/R13) when $C0=0$.
- The second one activates parity management in the C9/R9 test carried out in IVM when C0 reaches R1 (and which allows the positioning of the VMA update state when the $C9=R9$ condition on $C0=R1$ is verified)

The value of R5 is of little importance, **except on certain CRTC 1's** for the value **#10**.

This CRTC will be identified as 1-B while waiting to find out if the difference noticed really comes from the CRTC. The effect obtained by this value will be identified as **RFD#10**.

CRTC 1-A is defined as CRTC 1 which **does not support RFD#10**.

The additional management continues to be managed normally if R5 is not reset to 0 after the RFD has been triggered. If additional management is not desired for the screen, the reset of R5 can be done at any position of C0 after the activation of the RFD.

It is therefore possible to trigger an RFD via an "OUT R5,1", immediately followed by an "OUT R5,0" if it is only the RFD effect that is desired. If additional management and an RFD effect are desired, it is possible to do so by updating R5 once on $C0=R0$ with the number of additional rows desired.

Common processing of C4 versus C9 is not affected.

The RFD demonstrates that there is a state that allows CRTC 1 to accept consideration of R12/R13 at the start of the line regardless of the value of C4.

As a reminder, on the first character of a screen, VMA is assigned with R12/R13 and is loaded with VMA' on the other characters. VMA' is itself loaded with VMA when C9 reaches R9 and C0 reaches R1 (to account for the advance of the offset on the next row relative to the BORDER). The update of VMA with R12/R13 or VMA' takes place from $C0=0$.

VMA's update status via R12/R13 is usually true when $C4=0$, and then becomes false (VMA is then reloaded with VMA'). However, if for some reason the condition to test that the BORDER has been reached on the last line of the character **is not met**, then the VMA update status via R12/R13 remains true regardless of the value of C4.

It is important to note however that if the condition $C0=R1$ is not met (because $R1>R0$), then the condition $C9=R9$ is enough to deactivate the update of VMA with R12/R13. It is therefore not enough for $R1>R0$ to be able to modify the offset on each line.

RFD sets another status of the IVM interlace which involves screen parity in the C9=R9 equivalence. Thus, VMA update via R12/R13 is activated by the RFD and this state persists as long as the only true equivalence is $C0=R1$. However, the RFD does not modify the counting mode associated with the IVM mode.

In other words, this state remains active as long as the parity of the frame combined with the calculation mode of C9 comes into play on the comparative processing of C9. It is thus possible to end up with a situation equivalent to $R1 > R0$ (See Chapter 17.4.2) while $R1 < R0$.

The C9=R9 "out of parity" condition continues to be processed normally for the calculation of C4 and the reset of C9. The **RFD** does not affect the counting mode of C9 but determines the comparative values of C9 when C0=R1 activate VMA assignment with VMA' (instead of VMA=R12/R13).

11.5.1 RFD AND FRAME PARITY

The activation of an **RFD** implies a test of R9 carried out with the current parity.

On the **first screen (case 1)**, VMA' is no longer updated when C0 reaches R1 (because the test C9=R9 is faulty), and the characters are repeated. However, C4 continues to be managed whenever C9 reaches R9. VMA's update status is stuck on R12/R13, so it's possible to change the address on every line of every character, as if C4 was 0.

On the **second screen (case 2)**, VMA' is updated when C0 reaches R1 and C9=R9. Parity no longer corrupts the test and therefore characters do not repeat because VMA is updated with VMA'. On this screen, a R12/R13 update is no longer considered as soon as VMA has been updated with VMA' (so when C9=R9). A **RFD** triggered on the last line C9=R9 disables the state allowing VMA to be updated with R12/R13. However, the **RFD#10 of the CRTIC 1-B** always allows, when C9=R9, to deactivate the parity management in the test C9=R9 (See next Chapter).

C4 increments in both situations, because the screen remains perfectly synchronized on C4=R7.

The switching of parity, which takes place once each time the screen starts (C4=C9=C0=0 and R9 is odd), causes a stroboscopic effect between the two screens, except probably to position judiciously, at the right moment, $R1 > R0$ so that all rows repeat equally on both screens. But we will see that such a subterfuge is useless because there is something simpler.

11.5.2 IVM ON/OFF.

As we have just seen, the repetition of the first character on the screen defined as case 1 is the consequence of a fault in the equivalence test C9=R9 allowing the assignment of VMA' (and which locks the VMA update status). This C9 test involves screen parity. According to this parity, the test allowing VMA' assignment is assigned between each screen.

It is however possible to **fix the parity of a screen**, knowing that this **parity switches with each new screen** (or some other specific cases. see Chapter 19.5.3).

For example, it is enough to activate and deactivate the IVM mode with an **odd R9** to set an **even parity** (OUT R8,3 followed by OUT R8,0). I will name this action "**IVM ON/OFF**". See Chapter on IVM mode to discover the magic of an "**IVM ON/OFF**".

If an "**IVM ON/OFF**" takes place **before a RFD**, then all the screens will contain lines for which VMA' is no longer updated with VMA (case 1 mentioned in the previous Chapter).

In other words, **it is then possible to modify the offset on each line of the entire screen without any additional formality required.**

If an "IVM ON/OFF" takes place **after the RFD**, then all the screens will contain lines for which VMA' is updated each time C9=R9 (case 2 mentioned in the previous Chapter). In other words, it is possible to modify the offset until C9<>R9 from the line where the **RFD** is generated. The "IVM ON/OFF" having taken place after the R5 update, **it is on the new screen that the even parity will switch to become odd and cause this management from the second screen and the following.**

On **CRTC 1-B**, value #10 in R5 **deactivates parity management in test C9=R9**, while other values **activate this parity management (including value #10 on CRTC 1-A)** .

The brand and model of **CRTC 1-B** does not differ from other CRTC 1's (UM6845R).

This does not seem related to the batch number: the RFD#10 operates for example on a 6128 UM6845R-8804T, but not on a 6128 with UM6845R-8802T.

Out of 7 machines tested, 3 had this additional capacity.

If you want to identify this capacity on a CRTC 1, you can use SHAKER 2.1 by running the SHAKE21B.BIN module, test "O".

We can define that RFD:

- Activates a status authorizing the update of VMA with R12/R13 when C0 = 0 (this status is disabled when the test C9 = R9 on C0 = R1 is true).
- Active (or deactivates on the **CRTC 1-B** with RFD#10) a status authorizing the consideration of parity in the test C9 = R9 carried out when C0 = R1.

When the IVM state which authorizes the consideration of parity in the test C9 = R9 becomes active with a RFD, it is no longer possible to deactivate it until the screen is finished.

Therefore :

- If a RFD activates this status, an RFD#10 can no longer deactivate it.
- If a RFD #10 (**CRTC 1-B**) deactivates this status, a RFD "not #10" allows it to be reactivated.

Note 1: The "Sync Interlace" mode (IS ON/OFF) does not allow (to my knowledge) for fixing of the parity of the screen. The alteration of processing between each frame is not impacted if R8 changes between value 1 and 0 (or 2).

11.5.3 R.F.D. IN SUMMARY.

Method to change the video pointer on a character without having to worry about R4 or R7.

- On C0=R0, change R5 from 0 to 1 on any line different from C9=R9 for a C4 where the offset must be modified.
- OUT R5,1+OUT R5,0
- Modify R12/R13 on the line before the R5 update.
- Make R8 go from 3 to 0 once on an even C9 line.
- OUT R8,3+OUT R8,0

Method to change the address on each line.

- Wait for a new screen (C4=C9=0).
- Make R8 go from 3 to 0 once on an even C9 line.
- OUT R8,3+OUT R8,0
- On C0=R0, change R5 from 0 to 1 on any line 1 time for the screen.
- OUT R5,1+OUT R5,0
- Modify R12/R13 on the line preceding the one where the address must be modified.

This method is not a conventional RLAL, insofar as C9 participates in the construction of the video pointer. C9 is always 0 in RLAL. It is always possible to duplicate the video ram of the different C9s, but this implies a serious consumption of the ram according to the value of R9 programmed.

11.5.4 R.F.D. AND OTHERS CRTIC

Page 120 of the HITACHI technical guide (CRTIC 0) contains a table showing the anomalies that can occur when certain registers are modified during the display. Concerning R5, it is particularly indicated that if an update of R5 takes place on C0=R0, then there are "certain cases" where R5 is not really considered...Really ?

The contradictions in this table are a real playground!

11.6 R6 AND VERTICAL ADJUSTMENT

When C4 reaches R6, the display of the data is stopped.

On CRTIC 1 there is special management of R6 when it is 0, which allows for the activation of the BORDER in a non-definitive manner.

The technique which uses this management is called "split-border".

This technique is possible on CRTIC's 0, 3 and 4 using an R8 function (see Chapter 19.2.1, page 162).

This particular processing is managed in vertical adjustment.

11.7 INTERLACE ADJUSTMENT

In INTERLACE mode, a specific vertical adjustment management is carried out which results in an additional line in one of the two screens. See Chapter 19.3, page 167.

This adjustment occurs during "even" frames:

- On CRTIC 0 and 2, this adjustment is armed when C4=R6 when IVM is ON.

- On CRTC 1, the adjustment occurs when interlace is active.

The adjustment condition (interlace mode (IVM/Non IVM) activated and frame is even) is evaluated on the last line of a screen, when $C0=R0$, and only if R8 contains the correct value on the last line.

When the adjustment condition is met, the line is added as if R5 was $R5+1$.

12 COUNTING : REGISTER R4

12.1 GENERAL

The CRTC's R4 register defines the number of "character lines" to be displayed. A character-line is composed of several raster-lines, the number of which is fixed by the register R9. See Chapter 9.3.2, page 68

The line and character are numbered starting from 0.
The number programmed represents a value to be reached.

When all lines of a character are displayed ($C9=R9$), then C4 is incremented (the counter returns to 0 if C4 was R4 before being incremented).

The value of C4 is compared with R7 to trigger VSYNC and compared with R6 to trigger BORDER.

Note however that the Interlace mode of the CRTC delays the triggering of the VSYNC.

When $C4=R4$ and all the rows of the last character are displayed, additional row management can optionally begin if $R5 > 0$ or Interlace mode is enabled.

Note that with the exception of CRTC's 3 and 4, additional lines via R5 continue to increment C4 (which therefore exceeds R4 in this situation).

It should also be noted that this management of additional line(s) must be triggered when $R0 < 2$ on CRTC 0.

When C4 changes to 0 (and as long as it is 0 on CRTC 1), VMA is updated with R12/R13 content.

On CRTC 2 however, VMA is updated with VMA', which is itself updated with R12/R13 when $C0=R1$ from the last line (when $C9=R9$).

12.2 CRTC 0

When $C0=0$, the CRTC assesses whether $C9=R9$ and $C4=R4$ **to determine if it is on the last line of the screen**. It no longer repeats this test on the other values of C0.

It is not necessary to anticipate the programming of R4 on the previous line so that $C4=R4$ at the beginning of the next line. By positioning an OUT R4 on $C0vs=#3E$ (if $R0=#3F$), R4 is updated when $C0=0$ to satisfy the "**last line**" test. This allows compatibility with other CRTC's

If the CRTC has determined that it is on the last line of the screen, C4 will change to 0 no matter what happens (as well as C9). If R4 and / or R9 are modified during the line when $C0 > 1$ while it is **the last line, it does not change anything for C4 which will therefore return 0**.

If the CRTC determines that it is not on the last line (but that R9 was modified with C9), C4 will be incremented no matter what happens.

If R4 and/or R9 are updated during a line but **not the last line, it does not change anything for C4 which will be incremented** (when $C9=R9$)

When the last line of the screen is reached:

- Modifying R4 with C4 does not prevent C4 from incrementing if $C9=R9$ (if the goal was to increase it to 0).
- Modifying R4 with 0 while C4 is equal to R4 does not prevent C4 from returning to 0 (if the goal is to make it overflow).

The "last line" test is done at the beginning of the line, so it is necessary to anticipate the update of R4 and R9 according to what you want to achieve in C4.

Note that C9 can only overflow in a particular context (when $R0=0$).

The C4 counter can increment beyond the value set in R4 in several cases:

- If R4 is updated with a value less than C4 or has been incremented under the conditions described above, then C4 will "overflow". In other words, it will increment to its maximum value (127) before looping (if a new update of R4 does not occur before).
- C4 may also exceed the value of R4 when additional vertical line management is requested. This event can occur when $R5>0$ (or $R5=0$ with $R0<2$), or if INTERLACE mode is enabled on even screens (see Chapter 19.3, page 167). Note that if C4 exceeds R4 on at least one of these events, **it will return to 0 once the additional management is completed**

12.2.1 CASE STUDY : LINE-TO-LINE RUPTURE (R.L.A.L.)

The objective of this technique is to obtain consecutive lines for which $C9=C4=0$, in order to be able to modify the address via R12 and/or R13.

For the following two examples, the registers R4 and R9 are considered to be greater than 0.

From the first line of a screen:

If R9 and/or R4 are positioned at 0 when $C9=C4=0$, this line will not be considered the last on the screen (the test took place when $C0=0$).

On this second line, C4 will then be incremented ($C4 = 1$). And C9 will go to 0.

At the beginning of this second line, $C4(=1) < R4(=0)$. $C9=R9=0$.

The CRTIC will therefore increment C4 regardless of the value that is programmed in R4,...

If, on line 1, we program $R4=1$ and $R9=0$ (instead of $R4=0$ and $R9=0$), things will go better. If this line has not been considered the last, C4 will increment on the second line ($C4 = 1$) (and C9 will be equal to 0).

However, the test that took place at the beginning of line 2 indicates that it was the last one ($C4=R4=1$ and $C9=R9=0$). C4 will therefore increase to 0 on the third line.

But if we want this third line and all the others to be considered as the last, we must
... change R4 with 0 on the second line. And that's it.

From the last line of a screen ($C9=R9$ and $C4=R4$):

If R9 and R4 are updated to 0 when $C9=R9$ and $C4=R4$, this line is already considered the last. On the new line, C9 and C4 have both changed to 0, but not because of the modification of R9 or R4 or any "buffering".

At the beginning of this line between C0=0 and 1, the condition C9=R9=0 and C4=R4=0 is true. This line and the next ones will be considered as the last ones.

Note : When C9 becomes equal to R9 (last line), it is necessary to wait until C0=2 to modify R9, because CRTIC 0 requires special treatment with C0=0 and 1 to manage C9 and disable in particular the additional line management enabled by default.

C4:	0																			
C9:	7																			
C0:	0	1	2	3	4	5	6	7	8	9	10	11	12	...	58	59	60	61	62	63
R9:	7	7	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0
R4:	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0
	OUT R9,0														Update R12/R13 before C0=0					

How do we get out?

To stop getting lines C4=0 and C9=0, it is necessary to modify R4 and/or R9. Since each line is also a "last line", C4 and R9 will be reset to 0 on the next line, regardless of the update of R4 and/or R9. (Because C4 will be forced to 0, and de facto C9 also).

With a view to common code for CRTIC 2, it is advisable to:

- Modify R12/R13 before C0=R1.
- Manage the update of R9 during HSYNC as described in Chapter 12.4.1.
- Do not set R2=0 (so that the BORDER does not remain activated).

12.3 CRTIC 1

If R4 is updated with the value of C4:

- If we were on line C9 between 0 and R9-1, then C9=C9+1 (C4 will go to 0 when C9 goes back to 0 and the offset (R12/R13) will be considered).
- If we were on the last line (C9=R9), then C9 goes to 0, C4=0 and R12. R13 is considered.

If R4 is updated with a value less than C4, then C4 will increment to its maximum value (127) before looping back.

Unlike CRTIC 0, putting R4=0 on the last line of a screen will cause an "overflow" of C4, the value 0 being handled as a general case.

If we want to put R4 to 0 so that C4 loops to 0, we must do it only when C4 = 0.

Creating a line-to-line rupture on this CRTIC is trivial.

Simply set R4 and R9 to 0 when C4 and C9 are both at 0.

12.4 CRTIC 2

The CRTIC assesses, when C0=0, whether C9=R9 and C4=R4 to determine if it is on **the last line of the screen**.

When this condition is true, the CRTIC arms a reset of 0 for C4 for the next line (C9 goes to 0 systematically when C4 goes to 0). **If R4 and / or R9 are modified again during this last line, it does not change anything for C4 and C9 which will return to 0.**

A sneaky mechanism can however prevent C4 being reset to 0.

If a last line condition occurs at the beginning of a row, it is properly handled (unconditional reset of C4 and C9 to 0) for that row.

However, if the "**last line**" condition is still true **when C0 switches back to the last HSYNC character of the next line without C9 and R9 having changed**, then the last line state is **disarmed** and C4 will not be able to go back to 0.

If R9 is modified during this new "last line", C9 will be calculated in relation to this new value of R9.

If R9 is not modified (C9=R9) then C4 will be incremented unconditionally, regardless of the value of R4.

Also, it is enough to cancel the "**last line**" condition on the last character of the HSYNC to allow this CRTIC to manage the resetting to 0 of C4 as expected. **Modifying R9 wisely before and after HSYNC achieves this goal.**

When the CRTIC is not on the last line, R4 is considered immediately.

- C4 will be incremented if R9 is changed in the course of a line with the value of C9.
- C4 will revert to 0 if R4 is updated along the line with the value of C4 and C9=R9.

12.4.1 CASE STUDY: LINE-TO-LINE RUPTURE (R.L.A.L.)

The objective of this technique is that all the lines displayed start with C4=0 and C9=0, so that the registers R12 and R13 are modified before C0=R1 is considered.

Suppose we are on the **last line** of a screen with C4=R4 and C9=R9 (R4 and/or R9 are greater than 0). We know that on the next line, C9=0 and C4=0, but we want that for the next lines, C9 and C4 are also at 0 (and be able to change the address via R12 / R13).

It will be necessary to reprogram R9 and R4 with 0 so that the **last line** condition is active on each line. Each new line will be **a first and last line** of the screen.

For this example, the HSYNC will be positioned where C0=1 (via R2=1).

Consideration should be given to constraints related to other management flaws during HSYNC, such as not enabling the VSYNC pin and disabling the BORDER on C0=0.

We will consider that this HSYNC will have the minimum time necessary for a horizontal synchronization, namely 6 μ sec (via R3 = 6) because it will be necessary to modify R9 twice. This may as well be done as soon as possible when the index on the CRTIC register is already selected. If C9=C4=0 and the **last line** condition is true on the last character of the HSYNC, then the unconditional increment of C4 is armed. By modifying R9 during HSYNC so that the last line condition is false, it is possible to disarm this increment. By modifying R9 with a value other than that of C9, HSYNC processing can no longer corrupt C4 processing because its C9=R9 condition is no longer satisfied.

Once the HSYNC is complete, returning the value of R9 to the same as that of C9 (so 0), allows to indicate what the correct limit of C9 is, so that the condition "last line" is treated correctly.

Example with 3 lines:

1st line :

It is assumed here that C4=R4=0 and C9=R9=7, and the HSYNC is shown in orange :

	R2																			
C4:	0																			
C9:	7																			
C0:	0	1	2	3	4	5	6	7	8	9	10	11	12	...	58	59	60	61	62	63
C3:		1	2	3	4	5	6													R1
R9:	7	7	7	7	7	7	7	0	0	0	0	0	0	...	0	0	0	0	0	0
R4:	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0
	OUT R9,0																			
															Update R12/R13 before C0=R1					

This line is considered the last line on the screen because C9=R9 and C4=R4 when C0=0. This true condition in the HSYNC is not considered (to cancel the reset to 0 of C4) because during the previous HSYNC, C9 was 6 and R9 was 7 (false "last line" condition). R12 and/or R13 are modified before C0=R1 so that VMA' is updated with R12/R13 because we are... on the last line.

Note 1 : This assignment of R12/R13 depends on the "last line" state when C0=R1 (and not on the equality C4=R4 and C9=R9 which positions this state). This implies that changing R9 before equality C0=R1 does not prevent this assignment.

Note 2 : Changing R9=0 on this line allows for the next line to be considered a last line.

Note 3 : R9 must be updated from C0=1 in order for the last line condition to be true when C0=0. If R9 is changed to C0=0, then this line is not considered the last (0 is different from 7)(and therefore C4 will be incremented).

2nd line :

	R2																				
C4:	0																				
C9:	0																				
C0:	0	1	2	3	4	5	6	7	8	9	10	11	12	...	58	59	60	61	62	63	
C3:		1	2	3	4	5	6														R1
R9:	7	0	0	1	1	1	1	0	0	0	0	0	0	...	0	0	0	0	0	0	
R4:	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0	
	OUT R9,1				OUT R9,0				Update R12/R13 before C0=R1												

On C0=6 (last character of the HSYNC) the test C9(0)=R9(1) is false.
The increment of C4 is not armed because the requirement is not met.

The OUT R9,0 has the effect of modifying R9 when C0=7 and the HSYNC is finished.
On C0=7, the CRTC trigger the reset of C4 and C9 to 0 (condition of "last line" satisfied).

Note 1 : This reset to 0 of C9 (and C4) can then no longer be "cancelled".
If, in the example above an OUT R9,10 was added behind the OUT R9,0 (R9 would be updated with 10 on C0=11), it would not change anything for C9 and C4, which would return to 0 on the next line.

Thus, on the 3rd line we will have C9=R9=0 and C4=R4=0.

3rd ligne :

	R2																				
C4:	0																				
C9:	0																				
C0:	0	1	2	3	4	5	6	7	8	9	10	11	12	...	58	59	60	61	62	63	
C3:		1	2	3	4	5	6														R1
R9:	0	0	0	1	1	1	1	0	0	0	0	0	0	...	0	0	0	0	0	0	
R4:	0	0	0	0	0	0	0	0	0	0	0	0	0	...	0	0	0	0	0	0	
	OUT R9,1				OUT R9,0				Update R12/R13 before C0=R1												

This line is not a problem either, because the last line condition is again false on C0=6 (HSYNC) and true on C0=7 (Excluding HSYNC) (although it was true on C0=0, 1 and 2), which disarms the increment of C4 and arms its reset to 0. And so on...

Note 1 : For practical reasons it is perfectly possible to move the OUT R9,1 instruction by 4 µsec (on C0=4) (R9 is different from C9 on C0=R2+R3-1).

Finally, just as on CRTC 0 to "get out" of "last line" treatment, it must be remembered that when R9 is put back at a value greater than 0, this value is no longer considered if the CRTC considers that it is on a last line.

It will put C9 and C4 back to 0 on the next line, as CRTC 0 would.

If the last line condition was left active during the last HSYNC (there were two last lines with the same C9/R9), C9 will be treated in relation to the value of R9. C9 will be incremented if C9<>R9 as a CRTC 1 would, but C4 will be unconditionally incremented if C9=R9 (and C9 will return to 0).

With a view to common code for CRTC 0, it is advisable to:

- Treat the update of R9 on the last line as on the previous lines so that the next line is considered a last line, in order to ensure compatibility with the "last line" operation of the CRTC 0.
- Do not modify R9 before C0=2 for the same reasons.

12.5 CRTC 3, 4

If R4 is updated with the value of C4:

- If we were on the line C9 between 0 and R9-1, then $C9=C9+1$, C4 will go to 0 when C9 will return to 0 and the offset (R12/R13) is considered.
- If we were on the last line ($C9=R9$), then C9 goes to 0, C4=0 and R12/13 are considered.

The modification of register 4 is considered immediately at the end of the line.

If we want to put R4 to 0 so that C4 loops to 0, we must do it when $C4 = 0$.

If R4 is updated with a value less than C4, then there is overflow of the C4 counter. (unlike what happens with C9/R9).

It should also be noted that additional management of vertical lines does not increment C4 beyond R4 as occurs with CRTC's 0, 1 and 2.

Creating a line-to-line rupture on this CRTC is even more trivial than on CRTC 1, because you simply set R4 and R9 to 0 when $C4=0$.

Indeed, C9 increases to 0 if $C9>R9$ which improves the level of compatibility between CRTC's 0 and 1.

13 COUNTING : REGISTER R0

13.1 GENERAL

The CRTC's R0 register is used to define the number of characters which the circuit will generate on a line. A C0 counter (also called HCC by some eccentrics :-)) counts from 0 up to and including the value of R0. This register contains the desired number of CRTC characters per "line" minus 1.

When C0 is reset to 0, different counters are updated (C4, "C5", C9, ...).

The C0 counter is comparable to several other registers, such as R1 (border/video pointer management) and R2 (HSYNC management).

One might expect the condition $C_x=R_x$ to define the incrementing or resetting of other counters.

However, if C0 does not reach certain values defined internally, this poses some problems, especially on CRTC 0 because processing take place on specific values of C0.

The purpose of this processing is to allow the reset of counters or simply to manage the increment of other counters.

C0 is compared to R2 to define the start of the HSYNC. It is worth recalling that there is a discrepancy between the CRTC's internal registers and the actual display of the corresponding characters by the GATE ARRAY and/or ASIC. The CRTC counters are ahead of the GATE ARRAY display.

The GATE ARRAY does not respect this "shift" to generate the HSYNC's. Thus, the HSYNC occurs on the C0 of the "CRTC".

ASIC's, however, respect this delay to generate the HSYNC when the character corresponding to $C_0=R_2$ is displayed, which corresponds to C_0+1 of the CRTC.

13.2 CRTC 0

This CRTC performs operations on precise positions of C0 (arming resets and increments of counters, inhibition of processing).

The detail of this operation is necessary to better understand the specific processing of resetting C4 to 0, which only occurs when the CRTC assesses that it is on **the last line of the screen**.

The designers of the circuit probably "preferred" to manage under conditions a reset of C4, because this counter was planned to **exceed R4** on all CRTC's "not-ASIC'd".

This is particularly the case when R5 is greater than 0 (it then becomes the new limit of C9+1) or when the Interlace mode is active during an "even" screen.

These different "tests" were spread over several values of C0:

- **When C0=0**, then counters C4 and C9 are updated according to states decided on the previous line. Then the counters are evaluated to schedule their update on the next line. If C9 has reached R9 then C4 will be programmed to be incremented on the next line. If an additional management is in progress, then if C9 has reached R5, C9 returns to 0. Note that this evaluation of C9 takes place only once for the line (this management of C9 is deactivated once carried out). The incrementing of C4 will eventually be cancelled on C0=2 if this line was not the last on the screen (C4<>R4) or if there are additional lines to add (R5>0 and/or Interlace Line "on")
- **When C0=1**, then the management of C9 is again authorized for the next C0=R0. If this "authorization" is not given (context R0=0) then counter C9 is no longer managed on the next C0. If R0 is set to 0 on position C0=0, C9 is previously updated with respect to the last value of R9 if R0 of the previous line was >1.
- **When C0=2**, the CRTC determines if additional line management should take place. If this additional management is activated, then C4 will be incremented whatever the value of R4 for the next C0=0. Otherwise, both C4 and C9 will return to 0

Therefore :

- If **R0=0**, then C0 never reaches 1 (and therefore remains at 0) and **C9 can no longer count**. It then remains **frozen with the value it had before R0=0**.
 - If C9<>R9 on the first C0=0 for which R0=0, then **all of the CRTC counters are frozen** as long as R0=0. For example, freezing R0=0 for 64x8 µsec amounts to "forgetting" 8 lines (C4-1 if R9=7)
 - If C9=R9 on the first C0=0 for which R0=0, **then C4 is incremented once on the second C0=0**. C4 is only incremented once because the additional management is "deactivated" only on C0=2 (an additional management therefore only increments C4 once, because it deactivates the management C9=R9 to switch on C9+1=R5 management). After this second C0=0, **all of the CRTC counters are frozen as long as R0=0**.

Note 1 : Since C9 management takes place only once if C0 does not exceed 1, updates to registers R4, R5 and R9 are no longer considered as long as R0=0. On the other hand, R8 continues to be considered each time C0=0.

- If **R0=1**, then C0 never reaches 2, and the additional management of line(s) decided in C0=0 remains engaged if C4=R4 and C9=R9 on the previous character (C0=0). C9 can

increment according to R9. If R5=0, the additional management then lasts 1 line before ceasing (C4+1, C9=0). On the next line, the end of additional management reset C4 and C9 to 0.

The conditions for resetting C4 to 0 are therefore multiple :

- When C0=0, C4=R4 and C9=R9 conditions the "**last line**" state, which then activates an "**additional management**" state for which C4 is incremented unconditionally only once. Note that during this additional management, C9 continues to be tested with R9 for the update of VMA/VMA'.
- When C0=2, if there was no additional line pending, the additional management state is deactivated (R5=0 or "Interlace Line" allows it to be determined) which prevents C4 from being incremented for the addition of additional lines

Failing to meet all these conditions after C0>2, C4 will be incremented when C0 returns to 0. In other words, **modifying R4 or R9 after the tests are performed will not change anything regarding the C4 result.**

If the CRTIC was not on the last line (or having modified R4 or R9 before C0=0), the fate of C4 is already sealed: **C4=C4+1.**

FREEZE OF VSYNC...

Other operations take place on the CRTIC 0 between the values 0 and 2 of C0. Particularly to determine if a **VSYNC** will be authorized for the next occurrence of C0=0.

Each time C0=2, a state validates the update of C4=R7 on the next C0=0. This state is cancelled when C0=0.

Thus, if R0 is modified with a value lower than 2 on the line preceding the equivalence C4=R7 (On the line where C9=R9 and C4=R7-1), the VSYNC will not be authorized on C0=0. This will also cause the VSYNC to block for the value C4=R7.

A modification of R7 when C0<2 having the purpose of "triggering" a VSYNC after C0=0 (when C4<>R7) will also cause the blocking of the VSYNC for this value C4=R7.

Unblocking the **VSYNC** is then no longer possible for this value of C4, except for two specific conditions. See Chapter 15 for more description of these conditions.

FREEZE ON ADDITIONAL ADJUSTMENT

If an additional line is programmed (R5=1 for example), we will have on this line C4=R4+1 and C9=0. If R0 goes to 0 on C0=0 of this line, then C9 remains fixed at 0 and C4 can only go to 0 when C9 is managed again (as soon as C0=1).

C4 and C9 remain fixed as for a "non-additional" line for which C9<>R9. Modifying R5 for a period during which R0=0 has no effect on the value of the counters while C0 remains at 0, because C9 is no longer managed in relation to R5 as long as C0 has not returned to 1.

Note that when C9 management is inhibited, the update of both R9 and R4 are also ignored while R0=0.

FREEZE OF C9...

The fate of C9 is specific when $R0=0$ since it is no longer incremented.

On the first step of $C0=0$, when $R0$ becomes equal to 0, the value of C9 is calculated for the first time with respect to $R9$ (for example if C9 was worth 4 and $R9=7$, C9 goes to 5).

On the first $C0=0$:

- The CRTM manages different updated states on previous $C0=0,1,2$ to update C4 and C9 on $C0=0$. Each state is cancelled once the counter is updated. In principle, 4 states are possible :
 - Counting C4
 - Reset C4
 - Counting C9
 - Reset C9

Note that the processing of the status of C9 and its management of counting is subordinated to another status of 'management C9'.

- Tests are performed to determine the next states of C4/C9, specifically with respect to counting management C9/R9 or with respect to that of C9/R5 if additional management is decided (in this case, it is the value of R5 with respect to C0 which is used to set the end of the additional management)
- Additional management is decided if $C4=R4$ and $C9=R9$. It would in principle be confirmed on $C0=2$ if C0 managed to reach this value.
- C9 processing management is disabled. It would in principle be activated on $C0=1$ if C0 succeeded in reaching this value.

On the second $C0=0$

- The management of C9 has not been reactivated (because C0 has not reached 1). The value of C9 therefore remains the same as that which it had on the first " $C0=0$ "
- Two situations then arise :
 - If C9 had reached $R9$ on the first $C0=0$, then the reset of C9 had been armed as well as the increment to C4. With C9 being frozen, only C4 will increment.
 - If C9 was different from $R9$ on the first $C0=0$, then the increment to C9 will have been armed (but not the increment to C4). With C9 being frozen, no counter will have been moved.

On the third $C0=0$ (and the following ones) :

- The management of C9 has not been reactivated (because C0 has not reached 1). The value of C9 therefore remains the same as that which it had on the first " $C0=0$ ".
- In the situation where C4 has been incremented on the second " $C0=0$ ", this increment is deactivated because it has taken place. All counters are frozen.

Reminder : $R5$ is the quantity of line(s). It is therefore the value $C9+1$ which is compared with $R5$, while $R9$ is a value of C9 to be reached. $R5=0$ indicates that there is "in principle" no line.

If $R0$ is modified to become greater than 1 again, **increment management of C0 resumes normally** without the other counters being affected.

However, **if the conditions of a last line were satisfied during $C0=0$, then C9 will no longer be managed with $R9$ but with $R5$** . Going through $C0=2$ does not cancel it.

It will stop only when $C9+1=R5$ on $C0=0$.

The vertical adjustment management has 2 particularities on the CRTC 0:

- **C4 is incremented only once, whatever the value of R5.**
C4 returns to 0 once the adjustment is complete, whatever the value of R4.

This means that C4 is no longer managed when C9 reaches R9 during an additional management. Note however that the CRTC continues to manage VMA/VMA' transfers specific to C0=R1 when C9=R9. (See Chapter 11, page 75)

Note : On CRTC's 1, 2, 3 and 4, the "last line" assessment takes place during all C0 values, whereas CRTC 0 only manages it on C0=0 (and completes the status on C0=2). However, CRTC 2 arms a last-line reset to 0 that can no longer be disarmed afterwards, regardless of the values of R9 and R4. Respecting the strongest constraint, if R4 is changed so that its value is updated to C0=0 (OUT triggered on C0vs=#3E on CRTC's 0, 1, 2 and on #3D on CRTC's 3, 4 for R0=#3F) then only one instruction is required without adaptation to the code. If, however, it is also necessary to modify R9, which is part of the "last line" conditions, it is necessary to anticipate its update

See Chapter 12, page 84, and Chapter 10, page 68.

13.2.1 CASE STUDY: R0=1

When R0 is 1 (and C0<2) we obtain "lines" of 2 characters (2 µsec).

If C4=R4 and C9=R9 when C0=0, then we are potentially on the last line of the screen. But C0 not having reached 2, the additional line management is not disarmed and will take place.

If C4=R4 and C9=R9, then the "screen" ends when C0 reaches R0. This is particularly the case when R4 and R9 are 0, to create "screens" of 2 µsec. (The first line is then also the last)

Therefore :

- When C0=0, the CRTC assesses whether it is on the last line, and if so, arms an internal flag by default to trigger vertical adjustment.
- When C0=2, the CRTC assesses the conditions for disarming this vertical adjustment mechanism (in particular by testing the value of R5).

Consequently :

- If C0 never exceeds 1, and R4=R9=0, the CRTC generates a "1 line" vertical adjustment every "screen" when C4=R4 and C9=R9.
- The CRTC can no longer disarm the additional management (test of R5 and/or "Interlace on even frame programmed") and a 2 µsec "screen" is generated. This results in a one-time increment of C4 beyond the value programmed in R4. **However, the adjustment stops after 1 line.** For some reason I haven't determined yet, C9 (not C9+1) is compared to R5 to stop the adjustment.

Note: C4 and C9 return to 0 when the adjustment is complete

When R4=R9=0, each "line" of 2 µsec is therefore immediately followed by a "line" of 2 µsec for which C9=0 and C4=1.

Once this "additional" line of 2 µsec is completed, C4 and C9 reach 0 and the offset is updated. In this situation, the R12/R13 registers can therefore be considered "only" after 4 µsec, whereas this is possible every 2 µsec on a CRTC's 1, 2, 3 or 4 (and even 1 µsec when R0=0 on these CRTC's). If R9>0, this "line" of 2µsec (for which C4=1) occurs after the last value of C9 (when C9=R9).

13.2.2 CASE STUDY: R0=0

When R0 is 0 and C0=0, then C0 remains at 0 (screen or line of 1 µsec).

Things get a bit more complicated:

- C9 is frozen**
 Since C0 never reaches 1, C9 is no longer managed.
 If, for example, it was equal to 3 when R0 went to 0, it will remain at 3 regardless of the value of R9, as long as R0=0
- C4's last hiccup**
 If C9=R9 on C0=0 (when R0 goes to 0) then C9 is no longer managed, but C4 will however be incremented regardless of the value of R4. C4 is incremented without C9 returning to 0. **Magical !**
 After that, no more counter will be managed except C0.
- Additional management**
 If C9=R9 and C4=R4 (when R0 goes to 0), then we are in the same situation as in the previous paragraph, except that an additional management is activated, and which will remain so when C0 can once again exceed 1. It is then R5 which controls the end of the additional management. To stop this management, program R5 with C9+1

To summarize :

C9 remains "frozen" with the value it had before R0=0 and therefore no longer increments, nor returns to 0.

If C9=R9 and C4 <> R4 then C4=R4+1. When R0>0, C4 continues to be managed via C9/R9.

If C9=R9 and C4=R4 then C4=R4+1. When R0>0, C4 is managed by C9/R5.

In the other cases, C4 remains fixed

Example				
Context : C0=R0=C4=R4=C9=R9=R5=0				
	Counters	C0	C9	C4
1st character C0=0		0	0	0
The current video pointer is updated. CRTIC-VMA'=CRTIC-VMA=R12/R13 When C0 loops first time on R0, C0 goes from 0 to ... 0. C4=0. The CRTIC is at the end of the "screen" (it has just finished the R4/R9 lines of a 1 µsec screen (C4=R4/C9=R9))				
2nd character C0=0		0	0	1
C9=R9 and C4=R4. C4 is incremented (i.e. 1). We are on additional management. Note that C9 is not "really" reset to 0 because it is no longer managed.				
3rd character C0=0 (and next ones...)		0	0	1
The CRTIC is in additional management, but C9 is frozen.				
When R0 becomes > 2 again		0	0	1
The additional management being in progress, it can no longer be cancelled on C0=2 C9+1 will be compared to R5 on the next C0=0				
Next C0=0 after C0=R0>2		0	1	1
C9+1 being different from R5, then C9 is incremented.				
Example 2 (movie sequel)				
We will put R0=0 on the first C0 after C0=R0>2				
	Counters	C0	C9	C4
1st character C0=0		0	1	1
Take values from the end of the first example				
2nd character C0=0		0	1	1
C9 is frozen. Additional management is still ongoing.				

A BIT OF TECHNICAL STORY... THE R.V.I.

*Initially developed on CRTC 0 using a knife and string, an ancient ancestral technique called "RVI" (Invisible Vertical Rupture © Overflow) is intended to allow the choice of the C9 number of the visible line by creating small lines in the non-visible part of the screen (during HSYNC), while changing the address of the visible line. To achieve this, there are at least **3 different methods**, which can be combined: Either by modifying R9, or by changing the size of the lines (R0), or by limiting their number (synchronous action Z80A / CRTC). This allows you to individually control the address of many more rows than the 2k (among 16k of a page) allowed by the value C9=0*

*One of the major constraints of this technique is **the interdependence between the lines**. Also, you will really enjoy the next Chapter.*

Indeed, the value of C9 calculated for the new row displayed depends on the value of C9 of the previous row. Creating an algorithm that automatically determines the desired evolutions of C9 according to the current C9 further alters the CPU available on a line of 64 μ sec.

It is in principle the value of R9 that sets the maximum value of C9. It should be heeded that only the 3 bits of C9 are "preserved" for the composition of the address.

One of the corollaries of this technique is usually the update of CRTC-VMA via an update of R12 and / or R13. For this, it is necessary that C9 and C4 return to 0.

Note : For CRTC 2, it is also necessary for R12/R13 to be modified before C0=R1 and C0 reaches R1 when C9=R9, but you are not on the right Chapter.

*For example, if C9=8 corresponds to C9=0 for address constitution, C4 does not return to 0 and therefore R12/R13 cannot be taken into account. For a change of address to be considered, it is necessary that **C9 "loops" and returns to 0, as well as C4**. In addition, if the C9 displayed is a "last line", it will cause C9 to be reset to 0.*

Note : For CRTC 1, there is no need for C4 to go back to 0 for the address to be taken into account. This is true whenever C0=0 as long as C4=0.

When 2 μ sec screen-lines are created in the edge of the screen (or not if we want to expose the underside of the case ...) while R9>0, then C9 will increment until it reaches R9..

But in this situation, when C9=R9 (so here C0=1, since R0=1), an additional "line" will be generated with C4=1 and C9=0. This "additional" management results in the creation of an additional "line" when C9 reaches R9.

The change of address does not take place because C4=1. It is on the next line screen that C4 will return to 0 (with C9). One consequence is that the number of C9 increments for these "2 μ lines" is reduced by 1 compared to CRTC's 1, 2, 3, 4.

*This does not allow access, with R0 = 1, to C9 = 7 or 5 by changing the offset, because it is necessary on the one hand that **R9 is equal to 7 or 5, but also that it could have looped back to 0 before**.*

The final values of odd C9 do not help matters, unless you are a pro of the Interlace "controlled" (blah, blah, lawyer, blah, blah), but I digress...

As this technique was developed on CRTC 0, the use of R0=0 was quickly abandoned because of the difficulty in understanding the behaviour of counters at the time..

On CRTC's 1, 2, 3 and 4, this value (R0=0) is not a problem. Neither blocking C9 nor additional line C4=1, but it is more subtle for CRTC 2. It is therefore much simpler to create this type of rupture in the edge of the screen allowing access to all the values of C9 on the main line. The reset to 0 "triggered" on the "last line" is particularly interesting here compared to CRTC 1.

At first glance, the notion of "**last line**" on CRTC 0 (and 2) seems restrictive, because it does not allow "immediate" consideration of updates to the R4 and R9 registers.

In addition, CRTC 0 is limited to do rupture at least 2 µsec for "correct" operation of the C9 counter. Finally, if a "last line" occurs when this line is 2 µsec, then a new line of 2 µsec is generated (C4=1).

However, the principle of "**last line**" represents a great tool to **program in advance a reset of C4 and C9**, especially in the context of a vertical rupture, which I will call « Rupture Verticale Last Line » (in perfect Frenghish).

Indeed, if we consider that each visible line is a "last line", then **each first rupture of 2 µsec will be the first line of a screen with C4=C9=0**.

Thus, it is possible to anticipate the modification of R9 knowing that the next C9 will be equal to 0.

In this situation, the selection of the next C9 is greatly simplified since it is enough to set the desired number in R9 and create the appropriate number of ruptures (during HSYNC if the objective is to hide them) in order for C9 on the next line to be equal to that programmed in R9.

The update of the offset (R12/R13) then takes place during the first rupture of 2 µsec. Since the last line (C9=R9) is always the visible line larger than 2 µsec, the CRTC does not generate an additional rupture of 2 µsec.

This means that it takes 7 ruptures of 2 µsec to reach C9=7 (14 µsec in total).

This also means, except to cheat in a barbaric way with the value of the offset, that the rupture of 2 µsec begins essentially early in the 14 µsec in order to bring C9 to the desired value.

For this purpose, the value of R0 must therefore correspond to the moment when the ruptures of 2 µsec begin. Otherwise R0 must be equal to $63 - (R9 \times 2)$ (for $R9 > 1$).

In the diagram below the pink areas correspond to the OUT instructions on R0. R0-1 corresponds to the update of R0 at the beginning of the line (and therefore started at the end of the previous line), and R0-2 corresponds to the value of R0 for "hidden" ruptures.

R0-1	R0-2	R9	R2	OUT R0-2	OUT R0-1	New C9
63	x	0				
50	12	1				
59	1	2				
57	1	3				
55	1	4				
53	1	5				
51	1	6				
49	1	7				
CO:			...	47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	0
CO:			...	47 48 49 50 0 1 2 3 4 5 6 7 8 9 10	11 12	1
CO:			...	47 48 49 50 51 52 53 54 55 56 57 58 59 0 1	0 1	2
CO:			...	47 48 49 50 51 52 53 54 55 56 57 0 1 0 1	0 1	3
CO:			...	47 48 49 50 51 52 53 54 55 0 1 0 1 0 1	0 1	4
CO:			...	47 48 49 50 51 52 53 0 1 0 1 0 1 0 1	0 1	5
CO:			...	47 48 49 50 51 0 1 0 1 0 1 0 1 0 1	0 1	6
CO:			...	47 48 49 0 1 0 1 0 1 0 1 0 1 0 1	0 1	7
C3:			1	2 3 4 5 6 7 8 9 10 11 12 13 14 15		
						R3

Note : The 2nd OUT statement that begins on the 63rd character of the line is intended to resize the line for the next C9. This statement cannot start on the 64th character without causing C4 to overflow on the resized line (see Chapter 13.6.2).

On a CTM monitor, the visible part of a line is 48 μsec, and 16 μsec is not visible. However, for the screen to be centered, the HSYNC must start on the 51st character, when C0 reaches 50 (if R0=63). And so that R2 is programmed with this value.

To have the 14 μsec necessary to reach C9=7, R0 must be programmed with 49 and it would in principle be necessary that R2 is at 0 on this precise line (while inhibiting HSYNC by protecting the area with a value of R3 covering all other occurrences of C0=0).

A HSYNC is not necessary on each line, but it is possible to position R2 with 50, knowing that the lines C9=7 benefit from the synchronization of the other lines, but this implies that there are not several consecutive C9=7 lines. This is what is done in the R.V. demonstration provided with SHAKER, or lines 7 are out of sync. This is not a problem on native monitors.

To be able to use all the ram without this constraint, simply set R2=49. If C9=7 is not used, it is possible to set R2=50.

13.3 CRTIC 1

R0 accepts all values without causing any problem for other counters.

If R0 is 0, then C9 and R4 continue to be managed normally.

The offset can be modified according to the timings indicated in the diagrams of the following pages.

Note 1: It is possible to create 14 "hidden" ruptures, allowing to simply access all the values of C9, especially since the offset is considered while C4 = 0 (and not when it goes back to 0).

Note 2: The update of one of the offset registers taking at least 4 μsec, the only Z80A update instruction covers 4 "C0 line screens" when R0=0.

Note 3: Using the OUTI instruction to modify R0 when C4=C9=0 has unintended consequences compared to the same change made with an OUT(C),R8. The modification of the R0 register is effective on the 5th μsecond of the OUTI statement, and on the 3rd μsecond of the OUT(C),R8

instruction. As a result, the OUT(C),R8 instruction must begin 2 μ second later than the OUTI instruction. But in this circumstance, HSYNC or BORDER are affected. This bug having been reproduced on 2 different machines with a native CRTC 1.

I haven't yet fully defined what happens in this situation (in the next version of the document), but it does not imply either the position of the HSYNC (R2), nor the size of the line (R1), and it only takes place when a new "screen" starts on C0=0 when C4=C9=0 (On C0>0 there is no noticeable problem). The value of R0, however, has an importance on the bug and depending on the machine. I noticed a deterioration of the situation over time on one of my CPC's.

13.3.1 CASE STUDY : VERTICAL INVISIBLE RUPTURE (R.V.I.)

The R.V.I., on a CRTC 0, is very restrictive because placing R0 < 2 poses some constraints and limits the number of ruptures that can be made in the "invisible" part of the line. Indeed, when R0 is 1, an additional line is generated, and when R0 is 0, C9 is affected. This technique implies that C9 goes back to 0 so that R12 and / or R13 are considered, and this imperatively requires a high number of ruptures. It is impossible on CRTC 2, in particular because of the constraints of considering R12/R13.

When it comes to writing a program running on the CRTC's other than CRTC 0, the R0=0 value is not a particular problem. If the objective remains to access all C9, we will nevertheless prefer the R.V.L.L. on CRTC 0 and 2 which avoid a transitional management algorithm between the C9. CRTC's 1, 3 and 4 do not have this option.

CRTC 1, compared to CRTC 3 and 4 (and although CRTC 3 has many other ways to change the offset of each line) has an additional advantage to manage a R.V.I (if I have not already written it). Indeed, the offset is considered as long as C4=0, whatever the value of C9, unlike all other CRTC's. (See Chapter 20.3).

This allows the modification of the offset without C9 having "looped" to 0 and allows to limit the number of ruptures necessary to reach the desired C9 with a "new" offset, which allows for the placement of R2 at 50 for perfect screen centering.

The following tables describe the 64 transitional states between two C9. The method used involves updating R0 one or two times per line, as well as updating R9, R12 and/or R13.
A joy for all SudokuZ80A fans!

The values of the new C9s (shown in red) correspond to a CRTC 1 "C4=0" possibility. For CRTC 3 and 4, simply replace the values with those listed below each table. It should be noted that the passage C9=0 to 7 implies that R0 of the main line is equal to 49, limiting de facto the possibility of setting R2 to 50. This is not at all inconvenient for a CRTC 4, since it is the value that allows centering on this circuit. (See Chapter 16.1)

C9=0				R2	OUT R0.2	OUT R0.1	New C9								
Old C9	R0.1	R0.2	R9												
0	63		0	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	0								
0	63		1	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	1								
0	59	0	2	C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	2							
0	57	0	3	C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0	0 0	0 0	3						
0	55	0	4	C0:	... 47 48 49 50 51 52 53	54 55 0 0	0 0	0 0	0 0	4					
0	59	0	5	C0:	... 47 48 49 50 51 52 53	54 55 56 57	58 59 0 0	0 0	0 0	5					
0	58	0	6	C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	0 0	6						
0	57	0	7	C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0	0 0	0 0	7						

C3: 1 2 3 4 5 6

Compatibility CRTC 3 & 4			
Old C9	R0.1	R0.2	R9
0	59	0	1
0	53	0	5
0	51	0	6
0	49	0	7

R2	R3	New C9						
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	1				
C0:	... 47 48 49 50 51	52 53 0 0	0 0	0 0	0 0	5		
C0:	... 47 48 49	50 51 0 0	0 0	0 0	0 0	0 0	6	
C0:	... 47	48 49 0 0	0 0	0 0	0 0	0 0	0 0	7

C9=1				R2	OUT R0.2	OUT R0.1	New C9								
Old C9	R0.1	R0.2	R9												
1	63		1	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	0								
1	59	0	4	C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	1							
1	63		2	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	2								
1	58	0	3	C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	3							
1	56	0	4	C0:	... 47 48 49 50 51 52 53 54	55 56 0 0	0 0	0 0	4						
1	54	0	5	C0:	... 47 48 49 50 51 52	53 54 0 0	0 0	0 0	0 0	5					
1	59	0	6	C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	6							
1	58	0	7	C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	7							

C3: 1 2 3 4 5 6

Compatibility CRTC 3 & 4			
Old C9	R0.1	R0.2	R9
1	59	0	3
1	52	0	6
1	49	0	7

R2	R3	New C9					
C0:	... 47 48 49 50	51 52 53 54 55 56 57	58 59 0 0	0 0	2		
C0:	... 47 48 49 50	51 52 0 0	0 0	0 0	0 0	6	
C0:	... 47 48	49 50 0 0	0 0	0 0	0 0	0 0	7

C9=2				R2	OUT R0.2	OUT R0.1	New C9								
Old C9	R0.1	R0.2	R9												
2	63		2	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	0								
2	59	0	2	C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	1							
2	58	0	2	C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	2							
2	63		3	C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	3								
2	57	0	4	C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0	0 0	4							
2	55	0	5	C0:	... 47 48 49 50 51 52 53	54 55 0 0	0 0	0 0	5						
2	53	0	6	C0:	... 47 48 49 50 51	52 53 0 0	0 0	0 0	0 0	6					
2	59	0	7	C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	7							

C3: 1 2 3 4 5 6

Compatibility CRTC 3 & 4			
Old C9	R0.1	R0.2	R9
2	59	0	3
2	51	0	7

R2	R3	New C9				
C0:	... 47 48 49 50	51 52 53 54 55 56 57	58 59 0 0	0 0	3	
C0:	... 47 48 49	50 51 0 0	0 0	0 0	0 0	7

C9=3

Old C9	R0.1	R0.2	R9
3	63		3
3	58	0	3
3	57	0	3
3	56	0	3
3	63		4
3	56	0	5
3	54	0	6
3	52	0	7

	R2	OUT R0.2	OUT R0.1	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		0
C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0 0	0 0	1
C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0 0	0 0	2
C0:	... 47 48 49 50 51 52 53 54	55 56 0 0 0	0 0	3
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		4
C0:	... 47 48 49 50 51 52 53 54	55 56 0 0 0	0 0	5
C0:	... 47 48 49 50 51 52 53 54	0 0 0 0 0	0 0	6
C0:	... 47 48 49 50 51 52 0 0	0 0 0 0 0	0 0	7

C3:	1 2 3 4 5 6
	R3

Compatibility CRTC 3 & 4

Old C9	R0.1	R0.2	R9
3	58	0	4

	R2	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 0 0 0	0 0 0 4

C9=4

Old C9	R0.1	R0.2	R9
4	63		4
4	57	0	4
4	56	0	4
4	55	0	4
4	59	0	4
4	63		5
4	55	0	6
4	53	0	7

	R2	OUT R0.2	OUT R0.1	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		0
C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0 0	0 0	1
C0:	... 47 48 49 50 51 52 53 54	55 56 0 0 0	0 0	2
C0:	... 47 48 49 50 51 52 53	54 55 0 0 0	0 0	3
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	4
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		5
C0:	... 47 48 49 50 51 52 53	54 55 0 0 0	0 0	6
C0:	... 47 48 49 50 51 52 53 0 0	0 0 0 0 0	0 0	7

C3:	1 2 3 4 5 6
	R3

Compatibility CRTC 3 & 4

Old C9	R0.1	R0.2	R9
4	57	0	5

	R2	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57 0 0 0	0 0 0 5

C9=5

Old C9	R0.1	R0.2	R9
5	63		5
5	59	0	8
5	59	0	7
5	59	0	6
5	59	0	5
5	58	0	5
5	63		6
5	54	0	7

	R2	OUT R0.2	OUT R0.1	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		0
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0 0	0 0	1
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0 0	0 0	2
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0 0	0 0	3
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0 0	0 0	4
C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0 0	0 0	5
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		6
C0:	... 47 48 49 50 51 52 53 54 0 0	0 0 0 0 0	0 0	7

C3:	1 2 3 4 5 6
	R3

Compatibility CRTC 3 & 4

Old C9	R0.1	R0.2	R9
5	56	0	6

	R2	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 0 0 0	0 0 0 6

C9=6

Old C9	R0.1	R0.2	R9
6	63		6
6	59	0	9
6	59	0	8
6	59	0	7
6	59	0	6
6	58	0	6
6	57	0	6
6	63		7

	R2	OUT R0.2	OUT R0.1	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 60 61	62 63	0
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	1
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	2
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	3
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	4
C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	5
C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0	0 0	6
C0:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63		7

C3: 1 2 3 4 5 6

Compatibility CRTC 3 & 4			
Old C9	R0.1	R0.2	R9
6	55	0	7

	R2	R3	New C9	
C0:	... 47 48 49 50 51 52 53	54 55 0 0	0 0 0 0	7

C9=7

Old C9	R0.1	R0.2	R9
7	63		7
7	59	0	10
7	59	0	9
7	59	0	8
7	59	0	7
7	58	0	7
7	57	0	7
7	56	0	7

	R2	OUT R0.2	OUT R0.1	New C9
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 60 61	62 63	0
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	1
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	2
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	3
C0:	... 47 48 49 50 51 52 53 54 55 56 57	58 59 0 0	0 0	4
C0:	... 47 48 49 50 51 52 53 54 55 56	57 58 0 0	0 0	5
C0:	... 47 48 49 50 51 52 53 54 55	56 57 0 0	0 0	6
C0:	... 47 48 49 50 51 52 53 54	55 56 0 0	0 0 0	7

C3: 1 2 3 4 5 6

R3

13.4 CRTC 2

R0 accepts all values without causing any problem for other counters.

However, one of the peculiarities of this CRTC is to inhibit many treatments during HSYNC. See Chapters 15 (page 126) and 14 (page 114).

In particular :

- A GHOST VSYNC is generated when $C4=R7$ if this happens during the HSYNC. See Chapter 15 (page 126).
- C4's reset management (when on the last line of a screen) is disabled under certain conditions. See Chapters 12 (page 84) and 10 (page 68).
- The border deactivation condition (when $C0=0$) is also no longer supported, and the BORDER from the previous row remains active. See Chapter 14, page 114.

This CRTC displays 1 byte ($0.5\mu\text{sec}$) of BORDER before $C0=0$, but unlike CRTC 0, which does the same thing, the R8 SKEW DISP function does not exist to work around this problem. So, we cannot (to my knowledge) prevent the appearance of 1 byte of BORDER.

See Chapter 19, page 161.

R12/R13 content is "transferred" to CRTC-VMA' when $C0$ reaches R1.

Then CRTC-VMA' is transferred to CRTC-VMA at the beginning of the screen.

This implies that it is impossible to change offset if $C0$ does not reach R1.

See Chapter 14, page 114.

Changing the offset therefore implies that at least one microsecond of BORDER exists before $C0=R0$, so that $C0$ can be equal to R1.

The treatment of C4 and C9 on this CRTC partly follows the logic of CRTC 0, insofar as there is a notion of arming the reset to 0 or the increment of C4 on the condition of "**last line**". The CRTC determines if it is on a last line on the different positions of $C0$ and will arm the reset of C9 (and C4) to 0 for the next line, regardless of the values programmed after in R9 and R4 during the line. This notion is of paramount importance to enable the management of an RVLL on this CRTC.

When it is necessary to create the conditions allowing an offset change at each "line", C4, R4, C9, R9 must all be at 0 when $C0=0$, and $C0$ must have met R1 after R12 and/or R13 are updated.

Without a clever trick, C4 will overflow on the second line.

See Chapter 10.3.3, page 71.

If R0 is positioned at 3, for example, CRTC 2 will generate 16 "lines" of 4 μsec .

In this situation, care must be taken to ensure that R2 is greater than 0:

- So that HSYNC must start when $C0>0$ in for VSYNC to be considered when C4 reaches R7. However, this can be "bypassed".
- So that the BORDER is disabled (or at least does not remain enabled) when $C0=0$, which is a more annoying constraint.

13.4.1 CASE STUDY: VERTICAL RUPTURE LAST LINE (R.V.L.L.)

CRTC 2 collects an anthology of various constraints that must be considered if we want to achieve a vertical rupture...

Let's say it right away, performing a "traditional" RVI on this CRTC is impossible for a simple reason: For the offset update, C0 must reach R1 **on the last line. Modifying R12/R13 after C0>R1 does not allow consideration for the next line.** However, the RVI is based on the principle of reaching the last line in the invisible part of the screen, and it would therefore be necessary that a micro-line "in the edge" has a C0 that reaches R1 (when C9 = R9).

Setting R1=1 when R0=1 will activate the BORDER from C0=1. Unless you can modify R0 and R1 at the same time, not much more will be displayed....

It is therefore necessary that C0 can reach R1 on the visible line, which must also be the last of the screen. **This is good because RVLL works on this principle!**

CRTC 2 doesn't have any problem for the counting of C9 and C4 when R0=0. As such, it has the same potential for "hidden" ruptures as a CRTC 1, i.e. 14 ruptures of 1 µsec, which should have made it possible to solve the problem of centering encountered on CRTC 0, whose potential for hidden rupture is 7.

But unfortunately, this is only possible if 2 lines with identical C9 are not consecutive.

R0-1	R0-2	R9		R2	OUT R0-2	OUT R0-1	New C9
63		0	CO:	... 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61	62 63	0	
58	4	1	CO:	... 47 48 49 50 51 52 53 54 55 56 57 58 0 1 2	3 4	1	
57	2	2	CO:	... 47 48 49 50 51 52 53 54 55 56 57 0 1 2 0	1 2	2	
57	1	3	CO:	... 47 48 49 50 51 52 53 54 55 56 57 0 1 0 1	0 1	3	
55	1	4	CO:	... 47 48 49 50 51 52 53 54 55 0 1 0 1 0 1	0 1	4	
58	0	5	CO:	... 47 48 49 50 51 52 53 54 55 56 57 58 0 0 0	0 0	5	
57	0	6	CO:	... 47 48 49 50 51 52 53 54 55 56 57 0 0 0 0	0 0	6	
56	0	7	CO:	... 47 48 49 50 51 52 53 54 55 56 0 0 0 0 0	0 0	7	
			C3:	1 2 3 4 5 6			
					R3		

Like CRTC 0, there is a notion of "last line" to schedule an automatic reset to 0 of C9 and C4. However, this notion is not complete because this automatic reset to 0 is disabled if 2 consecutive HSYNC occur with the same C9=R9.

In other words, 2 lines with the same C9=R9 for 2 consecutive HSYNC cancel the reset to 0 of C4 (which then overflows dirty). It is impossible to modify R9 during HSYNC to prevent HSYNC from cancelling this reset to 0 (as can be done in a classic line-to-line rupture) because if you want to modify R9 during HSYNC, there is no magic trick to modify R0 in parallel to create hidden ruptures.

However, it is very useful to remember here that R9 is a 5-bit register of which only 3 bits participate to the video pointer. When line C9=8 is displayed, line C9=0 is displayed.

It is therefore possible to manage the contiguity constraints of the C9 using this principle, as can be seen in the following table:

R0-1	R0-2	R9		R2	OUT R0-2	OUT R0-1	New C9
55	0	8	CO:	... 47 48 49 50 51 52 53	54 55 0 0	0 0 0 0	8 (0)
54	0	9	CO:	... 47 48 49 50 51 52	53 54 0 0	0 0 0 0	9 (1)
53	0	10	CO:	... 47 48 49 50 51	52 53 0 0	0 0 0 0	10 (2)
52	0	11	CO:	... 47 48 49 50	51 52 0 0	0 0 0 0	11 (3)
51	0	12	CO:	... 47 48 49	50 51 0 0	0 0 0 0	12 (4)
50	0	13	CO:	... 47 48	49 50 0 0	0 0 0 0	13 (5)
49	0	14	CO:	... 47	48 49 0 0	0 0 0 0	14 (6)
48	0	15	CO:	... 47 48	0 0 0 0	0 0 0 0	15 (7)
			C3:	1 2 3 4 5 6			
					R3		

The demonstration provided with SHAKER uses a screen without identical contiguous C9 using all 8 blocks. However, the first and last lines use the "C9 and 7" principle in order to avoid this contiguity (by creating a line 0 via C9=8 and a line 1 via C9=9).

It should be noted, however, that to reach C9=6 and C9=7 (via C9=14 and 15), it is necessary for R0 to reach 49 and 48 respectively. This is not an ideal situation if the visible lines need to be centered.

The earlier C0=R2 occurs, the more "hidden ruptures" appear on the left side of the screen.

If you're curious you can watch the intro of "AMAZING DEMO 2021". A simple method to bypass the constraint of contiguous rows is to alternate 1 row out of 2 the table management of C9 to reach. Thus, a line 1 is then necessarily followed by a line C9 + 8 and the problem is solved.

Notes : Since CRTC 0 cannot create hidden ruptures of 1 µsec, this means that the first data to appear on the left is the 3rd byte of the line, followed by a 1/2 µsec of BORDER. On a CRTC 2, it would be the 1st byte of the line (when R0=0) followed by a 1/2 µsec of BORDER. Finally, on CRTC's 1, 3 and 4 in the same R2 context, it would be 2 bytes which would appear on the left.

13.5 CRTC 3, 4

R0 accepts all values without causing any problems for other counters.

If R0 is 0, then C9 and R4 continue to be managed normally.

The offset can be modified according to the timings indicated in the diagrams of the following pages, Chapter 13.7.

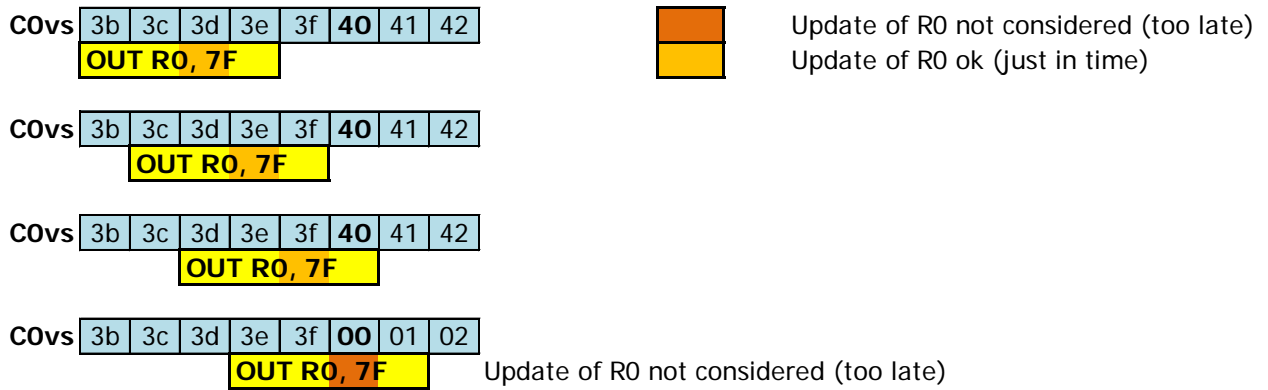
The techniques of R.V.L.L. are inapplicable on these CRTC's. The main "subtlety" of these CRTC's being the change from C9 to 0 if R9 is programmed with a value lower than the current C9 (which allows a "certain" compatibility with CRTC 0). It is possible to carry out an R.V.I. with the constraint of a loop from C9 to 0 so that the offset is considered. (See Chapter 13.3.1). Be careful, however, not to forget that the I/O takes place with 1 µs delay, which implies placing the OUT 1 µsec before those that would be done on a CRTC 1.

13.6 R0 UPDATE

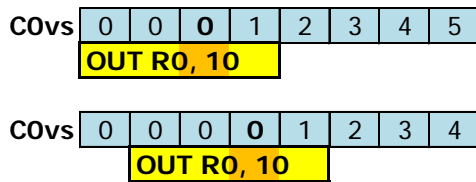
13.6.1 DELAYS

CRTC 0, 1, 2

Previous R0=#3f

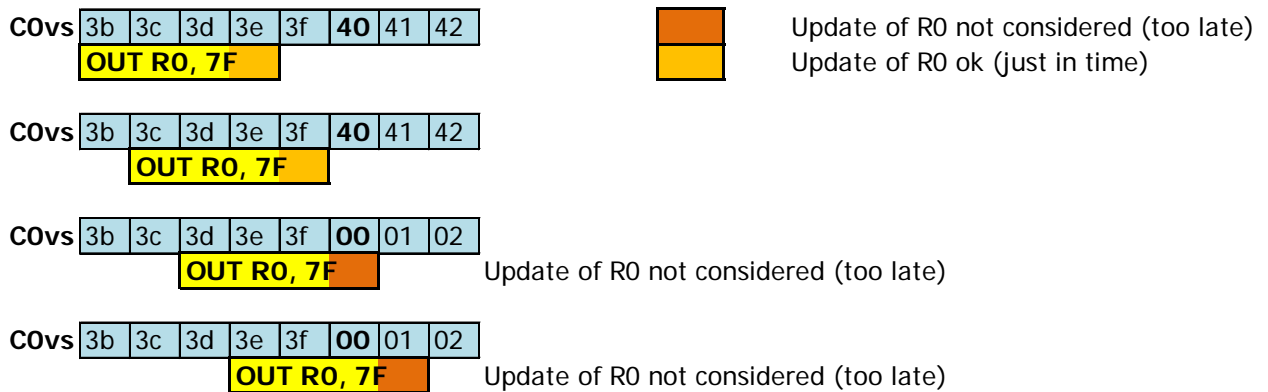


Previous R0=0

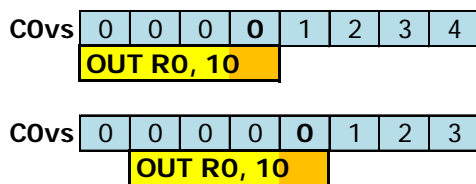


CRTC 3, 4

Previous R0=#3f



Previous R0=0



The update of the R0 register is considered immediately by the CRTIC for the counting of C0. The C0 counter never exceeds the value of R0 when R0 is updated according to the timing described in the previous diagrams.

That is, if R0=0 and C0 is 0, it will not overflow, and C0 will always be 0.

In general, the value programmed in R0 is 63 so that 64 μ sec flows before the counter goes back to 0. This loopback allows the C0 counter to return to the value of R2 in a period of 64 μ sec.

When R0 is reprogrammed during the line, it is necessary to plan to reprogram R2 so that the HSYNC takes place in the same place every 64 μ sec and that there is only one of more than 2 μ sec.

In principle, it is rather advisable to generate 1 HSYNC per line, but a CTM monitor will support not having 1 per line (blah, blah, heretics, blah, blah..., purists, blah, blah,...).

As previously stated, on CRTIC 0, updating R0 with a value of less than 2 prevents the CRTIC from carrying out certain specific treatments that have consequences on counting.

The minimum possible time between R13 and R12 (in this order) is 8 μ sec.
See Chapter 20, page 199.

13.6.2 EXCEPTIONS

There are certainly other exceptions that still remain to be established in a nice table but here are nevertheless some cases identified, according to the CRTC.

CRTC 1

There is a difference in CRTC 1's consideration of the update of R0 on a specific position of C0 according to Z80A instruction used for this update. The two instructions concerned are OUTI (I/O on the 5th μ sec) and OUT(C),reg8 (I/O on the 3rd μ sec). This reflects a difference in internal processing time at the level of the Z80A instructions.

This is the case when updating R0 to the position C0=0 when C4=C9=0. An RVI with ruptures of 1 NOP on this CRTC cannot use OUTI. See Chapter 13.3, page 99. I haven't (yet) identified exactly what is happening, but it seems to have an action on disabling the BORDER, and not on counting C0, having not noticed any desynchronization in this situation.

CRTC 0

When C0=R0, the CRTC will increment C4 if a reset to 0 has not been scheduled.

This reset of C4 is fully effective from C0=2 when the CRTC has assessed that it is on a last screen line (C4=C4 and C9=R9) and that there is no additional management (C9=R5, R8=1 or 3 and interlace line condition is ok, on the first frame where the register is updated on even C9).

Note that if an additional management is in progress, the reset to 0 is programmed and will normally occur at the end of this management.

To fully understand what I am going to describe, we must keep in mind that when the condition C0=R0 occurs after C0=2 **as part of additional management**, then C4 is incremented regardless of the value of R4, and C9 goes to 0 when C0 returns to 0. CRTC 0 saves C5 and uses C9 during additional management.

If R0 is programmed with a value of 1, then the additional management test is not performed, and the increment of C4 remains programmed when C9=R9. As part of the R0 update times, this management can be **partially accomplished** if the update takes place on C0 =1 while R0 = 1 and we want to modify it with a value greater than 1 (for example to pass a line to 64 μ sec ...).

If the update of R0 takes place when **C0=1 and C9=R9**, this causes an overflow of C4 without C0 and C9 being reset to 0, **even if C4 is not equal to R4**.

We are in additional line management when:

- C4 is unconditionally incremented.
- C9 can no longer go back to 0, even when C9=R9.

The C0=R0 test (with a value of 1) takes place before the register is updated, causing "additional management to begin". But the R0 register was however updated early enough to be taken into account for the increment of C0 as indicated in the previous Chapter (see Chapter 13.6.1) :

Screen Grid:	56	57	58	59	60	61	62	63	0	1	2	3	4	5	6	7	
C0:	...	56	57	58	59	0	1	0	1	0	1	2	3	4	5	6	7
R9=7 C9:	...	4	4	4	4	5	5	6	6	7	7	7	7	7	7	7	7
R4>=6 C4:	...	6	6	6	6	6	6	6	6	6	6	7	7	7	7	7	7

OUT R0,1

OUT R0,63

In this example, two situations are possible on the line C9=7 when R9=7 and when C0 reaches R0 (which is then 63 thanks to the second OUT).

13.6.2.1 We are not on a "last line of screen" (C4<>R4, C9=R9)

Additional management is automatically disabled on the C0=2 position (C4<>R4) because R5 is 0. The consequence is then just an overflow of C4 from C0 = 2, without C4 going back to 0 then as it would have done in additional management.

Note that this **overflow would not have occurred if C9 had been different from R9.**

In the example, C4 would have remained equal to 6.

C9/C4 counting control remains classic.

If, for example, it was necessary to compensate the two "lines" of 2 µsec created after C0=59 so that 8 complete lines would be displayed, it would be necessary to program R9 with 9 to add 2 new lines of 64 µsec.

13.6.2.2 We are on a "last line of screen" (C4=R4, C9=R9)

The last line status has been enabled with C4=R4, C9=R9, regardless of the value of R4.

This is also true if R4=0.

As in the previous case, C4 is incremented from C0=2.

Additional management is evaluated on the C0=2 position.

In this position, incrementing C4 without C9 returning to 0 **leaves the additional management activated.**

If, for example, it was necessary to compensate the two "lines" of 2 µsec created after C0=59 so that 8 complete lines were displayed, **it would be necessary to program R5 with 10** to add 2 new lines of 64 µsec. If R5 is not reprogrammed and was 0, C9 will increment to display lines 8 to 31, until it reaches R5. When the additional management is complete, then C4 returns to 0.

If we want to avoid that C4 is incremented during an "enlargement" of R0 which was 1, **it is therefore imperative to do it on the position C0 = 0.**

13.7 OFFSET ACCORDING TO C0

The following diagrams describe how to consider a change in offset (R12 and/or R13) from the current value of **C0vs**. CRTC 2 is not represented here as these tests were initially performed with an R1 value greater than R0.

Offset updates are represented with the colour green..

Initial data :

CRTC-R4=0

CRTC-R9=0

CRTC-R1=4

CRTC-R13=0

13.7.2 2 μsec SCREENS (R0=1)

CRTC 0

	R0																																																							
C4	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0	0																		
C0 from VSYNC	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																	
C0 from GA	24	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0																	
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																

The event C0 = R0 after 2 μsec leaves C4 = 1 for the 2nd period of 2 μsec, which represents a vertical adjustment "not canceled" (because C0 is never equal to 2)

CRTC 1

	R0																																																							
C4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																		
C0 from VSYNC	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																	
C0 from GA	24	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																

CRTC 3, 4

	R0																																																							
C4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0																		
C0 from VSYNC	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																	
C0 from GA	24	25	26	27	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																
	OUT R0 , 1																												OUT R13 , 4																											
C0 from GA/VRAM	x	x	x	x	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1																

14 SYNCHRONISATION : REGISTER R3

14.1 GENERAL

Register 3 may contain 2 different pieces of information, depending on the CRTC 6845 model.

In general, it allows to fix:

- The duration of HSYNC.
- The duration of VSYNC for some CRTC's.

In my various diagrams, I have represented the HSYNC using a counter C3 which starts at 1 on C0=R2 and which counts until it reaches the value of R3. Internally, the circuit most certainly counts from 0 and stops the HSYNC when C3=R3-1.

CRTC	7	6	5	4	3	2	1	0
0	Vsync	Vsync	Vsync	Vsync	Hsync	Hsync	Hsync	Hsync
1	x	x	x	x	Hsync	Hsync	Hsync	Hsync
2	x	x	x	x	Hsync	Hsync	Hsync	Hsync
3	Vsync	Vsync	Vsync	Vsync	Hsync	Hsync	Hsync	Hsync
4	Vsync	Vsync	Vsync	Vsync	Hsync	Hsync	Hsync	Hsync

Other CRTC	7	6	5	4	3	2	1	0
MC6845*1	Vsync	Vsync	Vsync	Vsync	Hsync	Hsync	Hsync	Hsync
UM6845E	Vsync	Vsync	Vsync	Vsync	Hsync	Hsync	Hsync	Hsync

Hsync CRTC				
0	0	0	0	No Hsync
0	0	0	1	1 nop
0	0	1	0	2 nop
0	0	1	1	3 nop
0	1	0	0	4 nop
0	1	0	1	5 nop
0	1	1	0	6 nop
0	1	1	1	7 nop
1	0	0	0	8 nop
1	0	0	1	9 nop
1	0	1	0	10 nop
1	0	1	1	11 nop
1	1	0	0	12 nop
1	1	0	1	13 nop
1	1	1	0	14 nop
1	1	1	1	15 nop

Hsync CRTC				
0	0	0	0	16 nop
0	0	0	1	1 nop
0	0	1	0	2 nop
0	0	1	1	3 nop
0	1	0	0	4 nop
0	1	0	1	5 nop
0	1	1	0	6 nop
0	1	1	1	7 nop
1	0	0	0	8 nop
1	0	0	1	9 nop
1	0	1	0	10 nop
1	0	1	1	11 nop
1	1	0	0	12 nop
1	1	0	1	13 nop
1	1	1	0	14 nop
1	1	1	1	15 nop

Vsync CRTC				
0	0	0	0	16 lines
0	0	0	1	1 line
0	0	1	0	2 lines
0	0	1	1	3 lines
0	1	0	0	4 lines
0	1	0	1	5 lines
0	1	1	0	6 lines
0	1	1	1	7 lines
1	0	0	0	8 lines
1	0	0	1	9 lines
1	0	1	0	10 lines
1	0	1	1	11 lines
1	1	0	0	12 lines
1	1	0	1	13 lines
1	1	1	0	14 lines
1	1	1	1	15 lines

14.2 VSYNC LENGTH

First-generation CRTC's generate a 16-line VSYNC.

The manufacturers have improved the circuit by adding a function to parameterize the number of lines, using the high-4 bits of R3.

In order to ensure compatibility of programs created for the first generation of circuits, the value 0 for the CRTC's integrating the new function corresponds to 16 lines of VSYNC.

The high-4 bits of R3 is used to indicate an exact number of lines, except for 0 therefore, which means 16 lines.

CPC ROM initializes VSYNC at 8 (R3=1000xxxx).

Thus, CRTC's 1 and 2, which do not manage these bits, generate 16 lines of VSYNC while CRTC's 0, 3 and 4 generate 8. (When R7 is already programmed before C4=R7).

Since CRTC's 1 and 2 do not know how to manage a configurable VSYNC, **it is advisable to avoid using this function** on CRTC's 0, 3 and 4 if the objective is compatibility. This can lead to incompatibilities for a program that would have the good idea to synchronize on the end of the VSYNC for example.

This involves systematically reprogramming this register because initialization by the rom creates a difference which could be avoided.

14.3 HSYNC GATE ARRAY VERSUS CRTC

When the GATE ARRAY receives a HSYNC signal from the CRTC, it stops the display for 2 µsec (approximately because it is possible to reduce this period) and then generates an HSYNC signal for the monitor whose maximum duration is 4 µsec. If the value programmed in R3 is greater than 6, the GATE ARRAY will display black for the remaining period.

If the HSYNC CRTC is greater than 6, then it does not affect the horizontal synchronization of the monitor. With a value less than 6, the HSYNC time for the monitor drops below 4 µsec.

The GATE ARRAY produces a composite synchronization signal used by the monitor. The HSYNC and VSYNC signals produced by the CRTC are merged into 1 single synchronization signal, which is present on pin 4 of the DIN6 video connector.

However, it can be useful to have a "CRTC" HSYNC greater than 6 because the CRTC does not consider the update of all its registers in the same way during this period and therefore makes it possible to inhibit processing.

Note : A short HSYNC may also have a discolouration effect on some non-CTM displays. This is for example the case if the CPC is connected to an ATARI SC1425 monitor (which was available with the ATARI 520STE). As indicated above, if the HSYNC is cut to 6 µsec (R3=6), the GATE ARRAY sends black for approximately 2 µsec followed by the HSYNC signal of 4 µsec. If the colour of the BORDER has been defined with something other than black (which an HSYNC longer than 6 would generate) this has a discolouration impact on the line because each colour component is

calibrated according to the colour present over the following 3 μsec (position 7, 8 and 9). If the BORDER is not black and $R3 < 9$, the colour will be affected on the line. On this type of monitor, it is therefore possible to obtain more colours.

14.4 HSYNC AND SCREEN POSITION

It is possible to use the HSYNC-GA size to shift the screen by about 1/2 character CRTIC (~ 1 byte). Since this "mechanism" is analog, the result depends on the setting of the CTM monitor and its tolerance.

Reducing the size of the HSYNC may produce, on screens other than CTMs, colour variations or unintended results.

The values used in general, without affecting the synchronization too much, are 5/6 or 4/5.

A value of 5 causes the image on the right to shift from a value of 6 (maximum value), regardless of the value of R2.

In the same logic, a value of 4 causes the image on the right to shift from a value of 5.

Note : On the game "Skatewars", Jon MENZIES uses the values &85 ,&8E, which is equivalent to the values 5/6 for the HSYNC-GA.

Continuously (and CPU-intensive) switching of these values between lines can reduce the offset size to 1/2 byte or create nice frames.

In this context, it is possible to do much better, since the **R3.JIT** technique can shift the end of the HSYNC by 0.25 μsec , therefore it's possible to obtain more combinations. Pixel scrolling in mode 1 is not a crazy idea...

14.5 HSYNC AND INTERRUPTIONS

Updating the HSYNC size changes when an interrupt is generated. The GATE ARRAY triggers an interrupt just after the HSYNC end, under certain conditions.

See Chapter 25, page 217.

14.6 UPDATING R3 DURING HSYNC

It is possible to change the value of R3 when C3 counts, which can affect the length of the HSYNC.

If R3 is changed with a value less than C3-1, then C3 is overflowing, **except for CRTIC 1 with a value of 0, which cancels the current HSYNC.**

If R3 is modified with the value of C3-1 at the time or C0 is on position C3, then the HSYNC is interrupted wildly. So, let's call this the **R3.JIT** technique.

The update of R3 during this count is considered according to the situations described below.

14.6.1 CRTC 0, 2

CRTC-R2=11 / CRTC-R3=10 (HBL Size = 10 chars)

		R2																						
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				Hsync-G Latency H/C Sync																				
				C3:																				
				1 2 3 4 5 6 7 8 9 10																				

		R2										OUT CRTC-R3, 0												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0																				

		R2										OUT CRTC-R3, 1												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1																				

		R2										OUT CRTC-R3, 2												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2																				

		R2										OUT CRTC-R3, 3												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 0 1 2 3																				

		R2										OUT CRTC-R3, 4												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5 (*)																				

		R2										OUT CRTC-R3, 5												
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29
				C3:																				
				1 2 3 4 5																				

	Z80A (OUT (C),r8) instruction
	Register update
	HSYNC Zone
	Characters displayed

(*) **R3.JIT** : The precise update of R3 interrupts the HSYNC after 0.25 µsec after its normal end if R3 had been programmed in advance. See next Chapters.

14.6.2 CRTC 1

CRTC-R2=11 / CRTC-R3=10 (HBL Size = 10 chars)

During an R3 update during HSYNC, CRTC 1 behaves like CRTC's 0 and 2, except when R3 is updated to 0. Indeed, the processing of R3=0 (no HSYNC) continues to be managed during HSYNC for this CRTC.

On CRTC's 0 and 2 in this condition, HSYNC continues and 0 is treated as a value to reach.

C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29									
Hsync-G		Latency		H/C Sync																													
C3:	1	2	3	4	5	6	7	8	9	10																							

		R2		OUT CRTC-R3, 0																													
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29									
C3:	1	2	3	4	5	(*)																											

		R2		OUT CRTC-R3, 1																													
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29									
C3:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1																

		R2		OUT CRTC-R3, 2																														
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30										
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29										
C3:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2																

		R2		OUT CRTC-R3, 3																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30											
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29											
C3:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3																

		R2		OUT CRTC-R3, 4																													
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29									
C3:	1	2	3	4	5	(*)																											

		R2		OUT CRTC-R3, 5																													
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29									
C3:	1	2	3	4	5																												

	Z80A (OUT (C),r8) instruction
	Register update
	HSYNC Zone
	Characters displayed

(*) **R3.JIT**. The precise update of R3 interrupts the HSYNC after 0.25 µsec after its normal end if R3 had been programmed in advance. See next Chapters.

14.6.3 CRTC 3, 4

CRTC-R2=11 / CRTC-R3=10 (HBL Size = 10 chars)

C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
Hsync-GA :		Latency		H/C Sync																															
C3:		1	2	3	4	5	6	7	8	9	10																								
		R2		OUT CRTC-R3, 0																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0																		
		R2		OUT CRTC-R3, 1																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1																	
		R2		OUT CRTC-R3, 2																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2																
		R2		OUT CRTC-R3, 3																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3															
		R2		OUT CRTC-R3, 4																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	0	1	2	3	4														
		R2		OUT CRTC-R3, 5																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5																													
		R2		OUT CRTC-R3, 6																															
C0 from Vcc :	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32									
C0 Displayed:	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31									
C3:		1	2	3	4	5	6																												

	Z80A (OUT (C),r8) instruction
	Register update
	HSYNC Zone
	Characters displayed

14.6.4 ZOOM ON R3.JIT

If R3 is modified via an **OUT(C),r8** with the value of C3-1 when C0 is at position C3 while R3 was greater than this value, then the **HSYNC** is wildly interrupted on CRTC's 0, 1 and 2. So let's call this technique **R3.JIT**

The use of OUTI does not allow this technique to be used on these CRTC's.

Whether with OUT(C),r8 or OUTI, this technique does not work on CRTC's 3 and 4, which synchronize the HSYNC with the display.

When a HSYNC starts, it does so at different positions depending on the CRTC's. See Chapter 14.8, 9.3.2.2 for more details on this subject.

The update of R3 can be carried out on all the positions of C0 during which the HSYNC takes place.

The first μ second of HSYNC is special, because interrupting it with the value 0 interrupts the HSYNC prematurely instead of delaying its end by 0.25 μ sec.

Note 1: Interrupting R3 with 0 using an OUTI simply prevents the HSYNC from starting.

However, the value R3=0 for a CRTC 2 means that the HSYNC will be 16 μ sec.

On **R3.JIT** with R3=0, the end of the HSYNC takes place after the last **Pixel-M2** of the current μ sec.

Note 2: On CRTC 1, in R3.NJIT (or with OUTI), the HSYNC ends 1 Pixel-M2 later than for CRTC 0 and 2.

On a CRTC 0, the HSYNC starts on the 5th pixel-M2 and lasts **4 pixel-M2's**.

On a CRTC 1, the HSYNC starts on the 6th pixel-M2 and lasts **3 pixel-M2's**.

The following diagrams describe the positioning of the HSYNC in **R3.JIT**.

The HSYNC is 1 pixel-M2 longer on the GA 40007 and 40008 compared to the GA 40010.

The possibility of mode change is indicated.

However, it must be considered that going from MODE 2 to another MODE "adds" 1 pixel M2 (9 pixels are generated from a byte) and going from MODE 0,1 or 3 to MODE 2 "subtracts" 1 pixel M2 (7 pixels are generated from one byte).

See Chapter 9.3.2 page 48.

14.6.4.1 R3.JIT ON CRTIC 0

C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	5th μ s OUTI (I/O R3=0)			
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	3rd μ s OUT (C),r8 (I/O R3=0)	4th μ s OUT (C),r8		
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	4th μ s OUTI	5th μ s OUTI (I/O R3=1)		
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=1)	4th μ s OUT (C),r8	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	3rd μ s OUTI	4th μ s OUTI	5th μ s OUTI (I/O R3=2)	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	1st μ s OUT (C),r8	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=2)	

14.6.4.2 R3.JIT ON CRTIC 2

C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	4th μ s OUTI	5th μ s OUTI (I/O R3=1)		
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=1)	4th μ s OUT (C),r8	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	3rd μ s OUTI	4th μ s OUTI	5th μ s OUTI (I/O R3=2)	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	1st μ s OUT (C),r8	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=2)	

14.6.4.3 R3.JIT ON CRTIC 1

C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	5th μ s OUTI (I/O R3=0)			
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	3rd μ s OUT (C),r8 (I/O R3=0)		4th μ s OUT (C),r8	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	4th μ s OUTI		5th μ s OUTI (I/O R3=1)	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=1)	4th μ s OUT (C),r8	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode Update
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	3rd μ s OUTI	4th μ s OUTI	5th μ s OUTI (I/O R3=2)	
C0	C0=R2	C0=R2+1	C0=R2+2	
40010	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode Update
40007/8	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Update
Z80a	1st μ s OUT (C),r8	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=2)	

14.6.4.4 R3.JIT ON CRTIC 4

C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	4th μ s OUTI		5th μ s OUTI (I/O R3=1)	
C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	
Z80a	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=1)	4th μ s OUT (C),r8	
C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode Update
Z80a	3rd μ s OUTI	4th μ s OUTI	5th μ s OUTI (I/O R3=2)	Ok
C0	C0=R2	C0=R2+1	C0=R2+2	
Pixel M2	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7 0 1 2 3 4 5 6 7	Mode Update
Z80a	1st μ s OUT (C),r8	2nd μ s OUT (C),r8	3rd μ s OUT (C),r8 (I/O R3=2)	Ok

14.7 ABSENCE OF HSYNC

When R3=0, CRTC's 0 and 1 do not produce HSYNC (**and therefore no interruption**).

On CRTC's 2, 3 and 4, it is impossible not to generate HSYNC if the C0=R2 condition is satisfied. A value of 0 in R3 will generate an HSYNC of 16 μ sec, unless it is interrupted by modifying R3 during HSYNC.

14.8 HSYNC START-UP

14.8.1 CRTC 0, 1, 2

When C0=R2 then a HSYNC is generated over a length of R3 characters. R2 update occurs during the 3rd μ sec of the OUT(C),reg8 instruction.

When the **update of R2 takes place before C0 reaches R2**, the HSYNC is processed by the GATE ARRAY during the display of the previous character, the character C0=R2 having not yet been displayed by the GATE ARRAY.

In this situation, the HSYNC black zone does not start exactly on a character boundary, and not at the same position according to the CRTC's.

- CRTC 0 : The non-display associated to the HSYNC starts from the start of the 5th mode 2 pixel after the start of the displayed CRTC R2-1 character. It was however observed the display of half of the 4th Pixel-M2.
- CRTC 1 : The non-display associated to the HSYNC starts from the start of the 6th mode 2 pixel after the start of the displayed CRTC R2-1 character.
- CRTC 2 : The non-display associated to the HSYNC starts from the start of the 4th mode 2 pixel after the start of the displayed CRTC R2-1 character. It was however observed the display of half of the 3rd Pixel-M2.

If the update of R2 occurs **while C0=R2** (during the 3rd μ sec of an OUT(C),r8) then the CRTC sends the HSYNC signal later to the GATE ARRAY. This reflects a delay between the execution of the instruction in Z80A and the consideration by the CRTC.

However, if this update is performed via the OUTI instruction (during the 5th μ sec of the instruction) then the HSYNC signal is sent faster to the GATE ARRAY by 0.25 μ sec, which then behaves as if R2 had been programmed before that C0=R2.

A **R2.JIT** ("Just In Time") update performed with an OUT(C),r8 causes the HSYNC black zone to appear later than in other situations (R2 programmed before C0=R2 or i/o OUTI on C0=R2)

In this situation, the stop position of the display depends on the type of CRTC:

- CRTC 0, 1: The non-display associated to the HSYNC starts from the start of the 9th mode 2 pixel after the start of the displayed CRTC R2-1 character. It was however observed the display of half of the 8th Pixel-M2.
- CRTC 2: The non-display associated to the HSYNC starts from the start of the 8th mode 2 pixel after the start of the displayed CRTC R2-1 character. It was however observed the display of half of the 7th Pixel-M2.

The HSYNC duration remains counted down with the value programmed in R3 (unless R3 is modified during the HSYNC). The delayed display of the HSYNC black zone does not change the synchronization of the monitor with respect to an anticipated R2 programming.

This special case of update (**R2.JIT**) allows delaying of the start of the displayed HSYNC by 4 mode 2 pixels (i.e. 0.25 μ sec) (1 T-State) on CRTC's 0 and 2, and 3 mode 2 pixels (0.1875 μ sec) on CRTC 1.

This technique allows delaying of the end of display by the GATE ARRAY of the black zone from 0.1875 to 0.25 μ sec. This is interesting in the event of a change of graphic mode during a line to limit the area of absence of display. It should nevertheless be considered that mode 2 is displayed 1 pixel (0.0625 μ sec) earlier by the GATE ARRAY than for the other graphic modes.

On the diagrams on the following pages, R3 is fixed at 2.
R2 before modification is greater than 10.

14.8.2 CRTC 3, 4

When $C0vs=R2$ then an HSYNC will be generated.

This update is considered in order to correspond to the display of the character corresponding to C0 by the GATE ARRAY, but the test is nevertheless carried out with respect to C0vs.

An **R2.JIT** ("Just In Time") update carried out with an OUT(C),r8 does not cause the HSYNC black zone to appear later than in the other situations since the HSYNC is deferred.

The CRTC 4 ASIC simulates the GATE ARRAY, insofar as the display of pixels in mode 2 begins 1 Pixel-M2 before the display of pixels in the other graphics modes.

On this CRTC, the display stop linked to the HSYNC starts from the 19th mode 2 pixel after the start of the displayed CRTC R2-1 character. However, the display of half of this 19th Pixel-M2 pixel was observed.

As a reminder, an I/O via an OUT(C),r8 takes place during the 4th μ sec of the instruction on CRTC's 3 and 4. An I/O on the OUTI instruction takes place during the 5th μ second of the instruction, as for other CRTC's.

The diagrams below illustrate the previous remarks by showing the positioning of the HSYNC according to the moment when the update of R2 takes place and according to the instruction used.

The CRTC 3 diagram will be added in a later version. Currently assumed to be the same as CRTC 4, but with HSYNC starting on the 17th pixel after the start of the displayed CRTC R2-1 character.

15 SYNCHRONIZATION : REGISTER R7

15.1 GENERAL

The R7 register is used to fix the moment when the CRTC generates its VSYNC signal. This signal is sent to the GATE ARRAY.

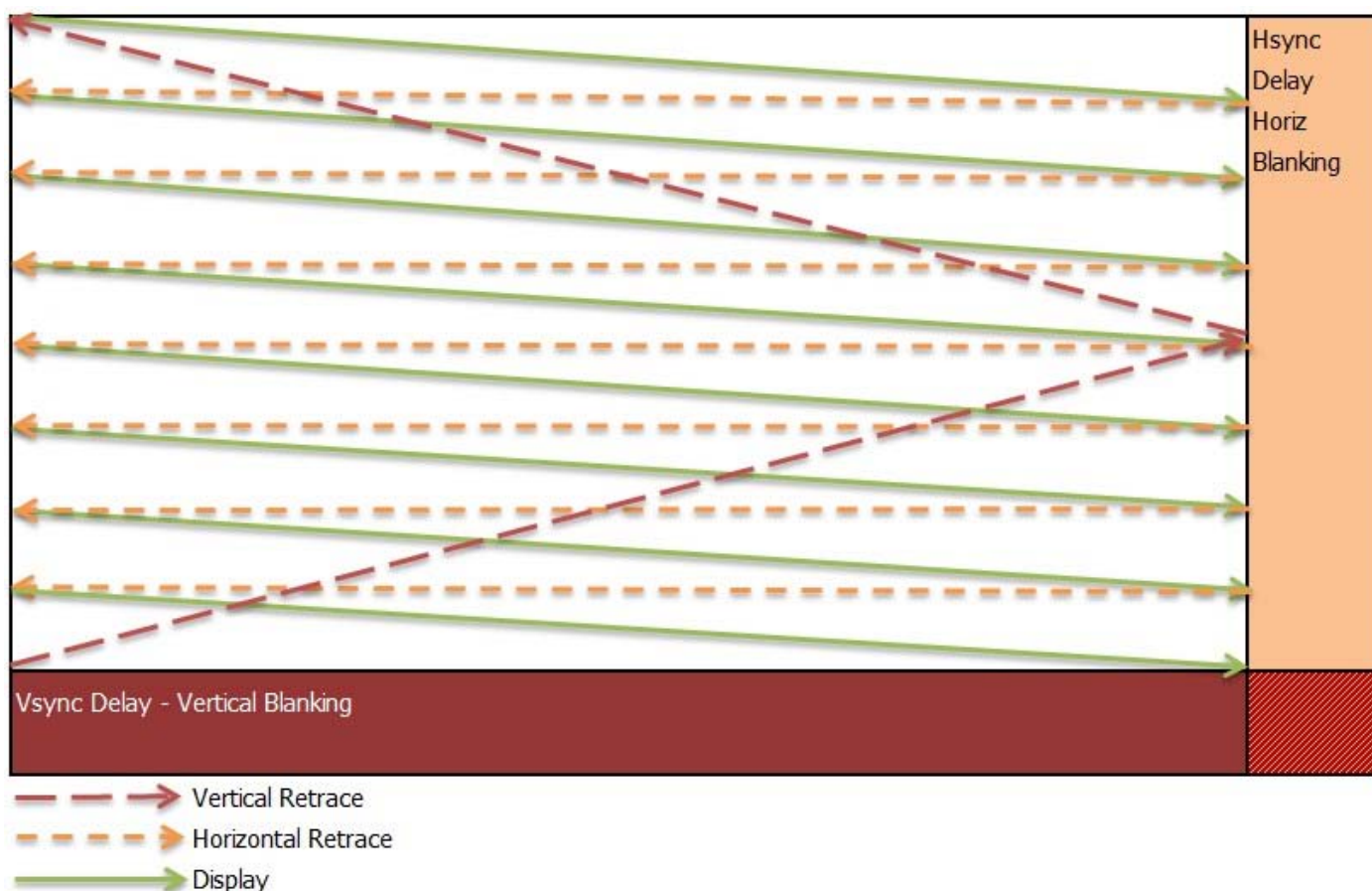
This signal is generally sent when $C4=R7$.

When the VSYNC CRTC starts, the GATE ARRAY counts the number of HSYNCs encountered.

At the end of the 2nd HSYNC, the GATE ARRAY sends its VSYNC signal to the monitor

Note : This counting of HSYNC by the GATE ARRAY takes place whatever the size of the HSYNC encountered. If for example, $R3=1$ after the start of the VSYNC, the 1 μsec HSYNCs encountered when $C0=R2$ will update the HSYNC counter of the GATE ARRAY

It is from the VSYNC signal sent by the GATE ARRAY that the monitor beam rises diagonally upwards, zigzagging to reposition itself on the character where the signal was received from the GATE ARRAY.



The vertical deflector of the monitor constantly descends at a constant speed. Although deliberately exaggerated in the diagram above, the beam descends when displaying the image from left to right. This cannot be seen thanks to internal tilt adjustments. This phenomenon is less noticeable when the beam returns from right to left because the horizontal deflector goes faster during a HBL and the slope is less.

During the VSYNC period, the GATE ARRAY does not display a character, but the CRTC continues to manage its counters and pointers. This physical return of the electron beam by the monitor is also called Vertical Blanking Line (VBL). Unlike the latency period during which the GATE ARRAY generates a black colour, the VBL period represents a real absence of display.

The size of the VSYNC is expressed in number of HSYNC's.

This number of HSYNC's is programmable on CRTC's 0, 3 and 4 (via register R3) and is fixed at 16 for CRTC's 1 and 2.

As with HSYNC's, it is possible to generate several VSYNC's during a frame, but the monitor will only be able to lock onto a VSYNC signal.

It is not possible to trigger or inhibit a VSYNC during a VSYNC. Thus, modifying the value of R7 with a value of C4 reached during the VSYNC does not cause a new VSYNC. Modifying R7 with a C4 value different from the initial C4 value does not interrupt the current VSYNC.

Finally, on a CTM monitor, the image begins to be visible from the 34th line (which represents the second line of the 5th character of 8 lines from the start of the VSYNC).

15.2 CONDITIONS TO CONSIDER

15.2.1 CRTC 0

VSYNC CRTC starts when $C4=R7$.

If C4 becomes equal to R7 when $C0vs$ reaches 0, then the VSYNC starts on $C0vs=0$.

15.2.1.1 R7 Update

If R7 is modified with the value of C4, then the VSYNC is triggered immediately if it was not already in progress, **except if this modification occurs when $C0vs=0$ or $C0vs=1$.**

If the modification of R7 with the value of C4 took place when $C0vs < 2$, we are in a **BLOCKED VSYNC** situation FOR C4. This means that the VSYNC can no longer occur on the value of $C4=R7$ until an unblocking situation is produced.

For $R7=C4$ updates when $C0vs > 1$, the VSYNC is "triggered" during the line.

In this case, the row counter starts with 0.

This VSYNC line counter is initialized at the start of the next line when $C0=0$.

Any line of the VSYNC is affected by this mid-line start.

Therefore, the total duration of the VSYNC is increased by the number of μsec corresponding to the calculation $R0 - C0vs$ (from the moment when R7 was updated).

So if a VSYNC is triggered during line number 1, then the VSYNC ends at the end of line 17.

Examples :

- If R7 is modified on $C0vs=\#36$, then the next read of the PPI-PORT B (read 6 μsec later on $C0vs=\#3C$) returns an active status of the VSYNC.
- If R7 is modified on $C0vs=\#00$, then the next read of the PPI-PORT B (read 6 μsec later on $C0vs=\#06$) returns an inactive status of the VSYNC

15.2.1.2 R0 UPDATE

The counter C0 needs to reach the value 2 on the line preceding that where C4=R7 for a VSYNC to be validated. Thus, if the length of the previous line is limited to 0 or 1 μ sec (R0=0/1), the VSYNC will be blocked for C4=R7 of the current line as long as an unblocking situation has not occurred.

15.2.1.3 Unblocking VSYNC CRTC

When a VSYNC is blocked in the two scenarios mentioned above, there are two conditions for unblocking allowing a VSYNC to occur again:

- C4 must change value. It should be specified here that it is not a question of a new calculation C4 when C9=R9 but of a modification of its value. Indeed, if we are in the context of a **BLOCKED VSYNC** when R4=0 (R7 has been modified with 0 when C4=0 and C0=0 or 1), then C4 will remain at 0 each time C9=R9, but no more VSYNC will be able to occur.
- C4<>R7 when C9 returns to 0 after reaching R9. So, if C4=R4=0, updating R7 with a value different from 0 will unlock the VSYNC.

As a reminder, a started VSYNC can no longer be stopped before its end.

15.2.2 CRTC 1

VSYNC starts when C4=R7.

If R7 is modified with the value of C4, then VSYNC is triggered immediately.

If R7 is modified when C0vs=#36, for example, then the next reading of the PPI (at the earliest 5 μ sec after, so on C0=#3B) returns an active status of the VSYNC.

The "triggered" activation of the VSYNC counts the line as if the VSYNC had started when C0=0.

As a result, the total VSYNC duration is reduced by the number of μ sec corresponding to the value of C0+1 from the moment R7 was updated.

If a VSYNC is triggered during line number 1, then the VSYNC ends at the end of line 16

15.2.3 CRTC 2

VSYNC is considered on all values of C0 and C9 when C4=R7, but also on C0=R0 of the previous line C4=R7 (when C9=R9). If an HSYNC occurs when the first VSYNC condition is evaluated, then the CRTC generates a **GHOST VSYNC**.

If R7 is modified with the value of C4, then the VSYNC is triggered immediately, except during HSYNC, which triggers the **GHOST VSYNC**.

A **GHOST VSYNC** means that the CRTC counts the lines as if a VSYNC were taking place by preventing a new VSYNC from occurring, but without the VSYNC pin being enabled.

The "triggered" activation of the VSYNC counts the line as if the VSYNC had started in C0=0.

As a result, the total VSYNC duration is reduced by the number of μ sec corresponding to the value of C0+1 from the moment when R7 was updated

If a VSYNC is triggered during line number 1, then the VSYNC ends at the end of line 16.

To get around the problem of no VSYNC on this CRTIC, just avoid generating a **GHOST VSYNC**. Thus, by positioning R7 far into the cosmos (e.g. 127), it is then sufficient to update R7 with C4 when C0 is no longer present in the HSYNC period of the line considered

15.2.4 CRTIC 3, 4

VSYNC starts when $C4=R7$ and $C9=C0=0$.

If R7 is modified with the value of C4 while $C0>0$, it will not trigger VSYNC.

15.3 LIMITLESS VSYNC !

In a system without a GATE ARRAY, if the VSYNC signal from a CRTC was sent directly to the monitor, the monitor would be able to start its return phase to the top of the monitor to satisfy the constraints of the interlaced mode.

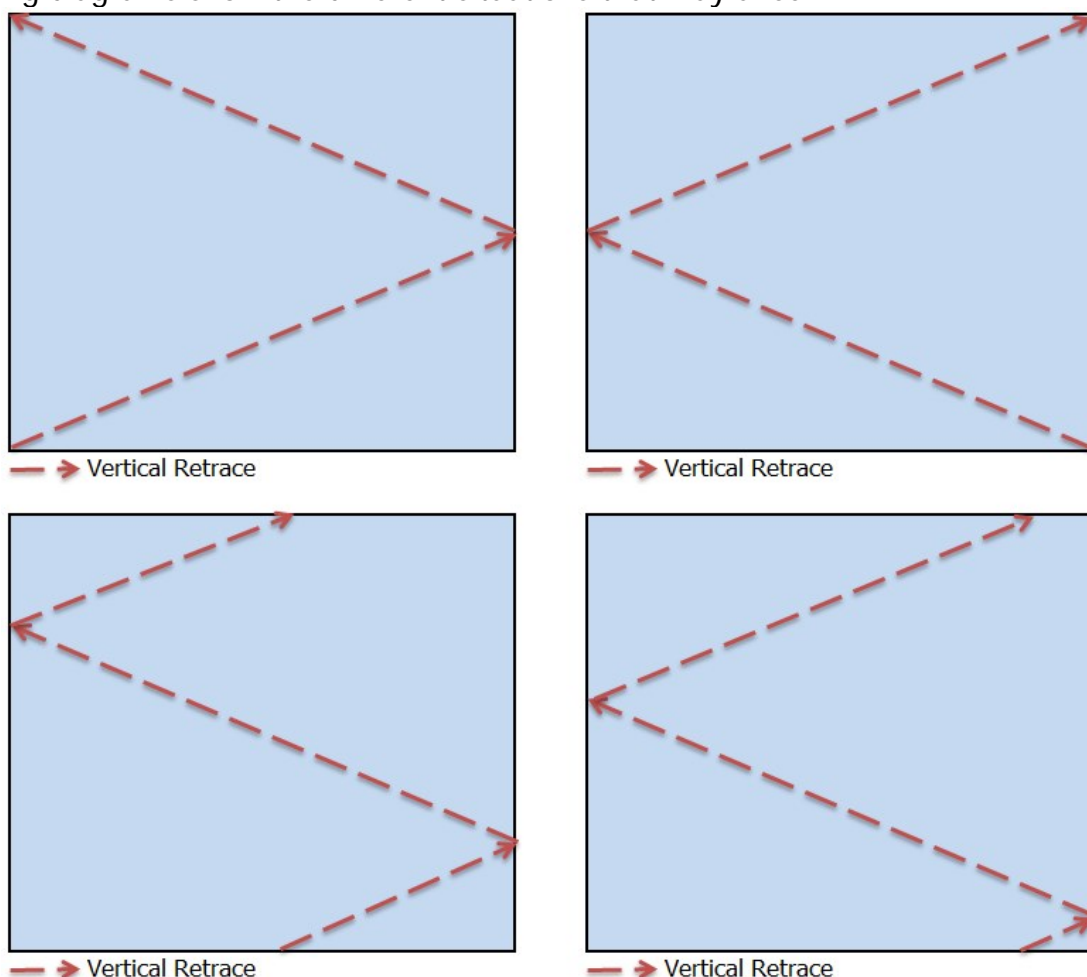
As part of an image composed of 2 frames, the CRTC in Interlace mode generates an odd and even screen of 312 lines each, separated by a line on which the VSYNC will be generated in the middle of the line ($R0/2$). See Chapter 19.3, page 167.

Unfortunately (or fortunately, we are going to see it) it is the GATE ARRAY which filters the HSYNC and VSYNC signals from the CRTC and which generates a mixed signal HSYNC+VSYNC towards the monitor as soon as it arrives on the 2nd HSYNC which follows the VSYNC generated by the CRTC. It thus short-circuits the "native" timing of the CRTC's for "Interlace" operation.

It is still possible to force the GATE ARRAY to send the VSYNC signal to the monitor at the right time if you want to obtain an "interlace" image. It suffices for this to place the 2nd HSYNC which occurs after the VSYNC CRTC at half the distance from the line compared to that which usually takes place (i.e. a delay of $R0/2 \mu\text{sec}$). However, we must not forget to compensate the deficit thus created for the CTM. It is therefore possible to display an "interlace" image quite simply.

The beam rises diagonally to reach the horizontal position left at the bottom of the screen. Depending on the horizontal position of the beam when the request is made, the latter zigzags to reach the horizontal position it has just left.

The following diagrams show the different situations that may arise.

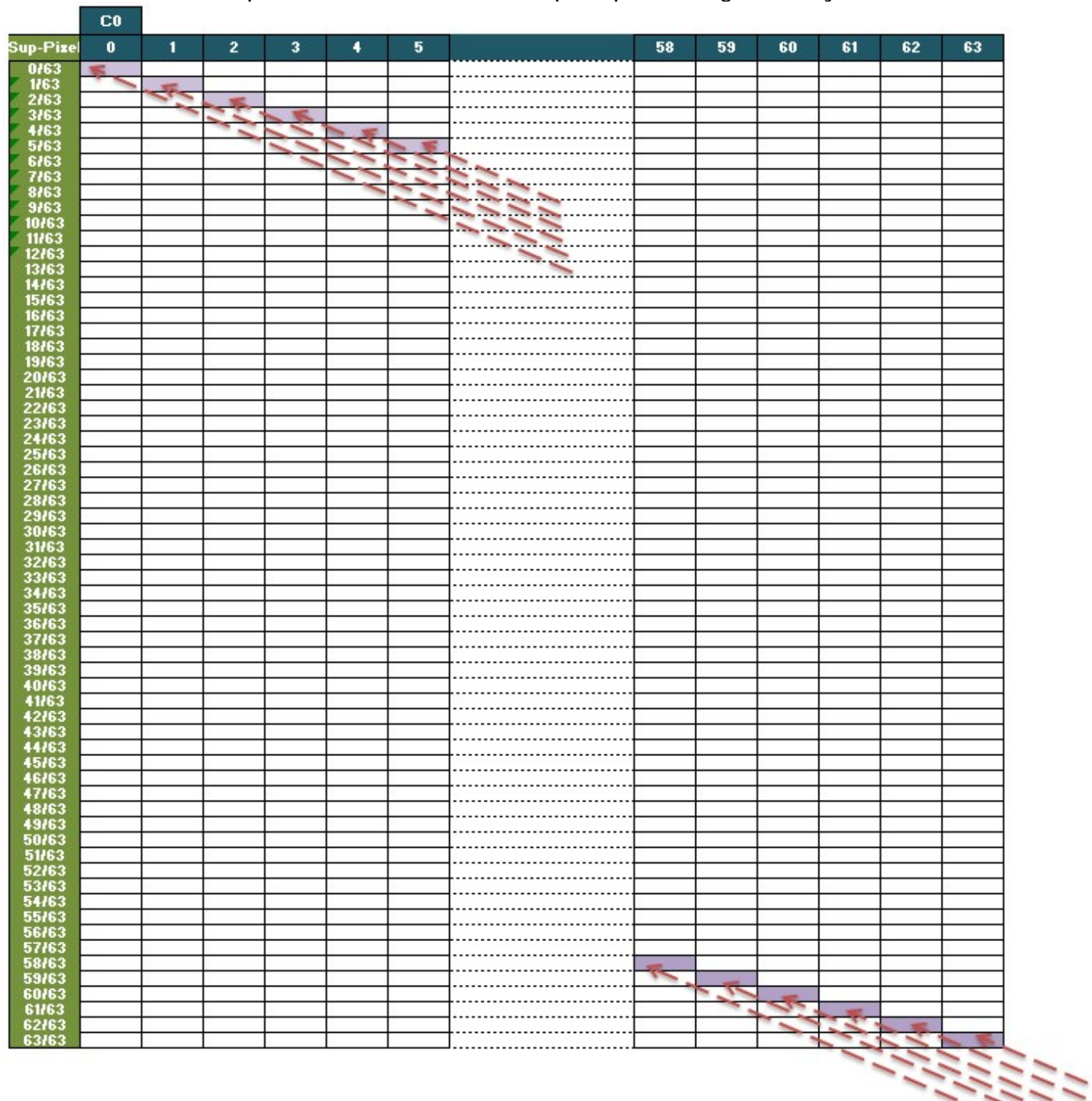


The later the beam starts, the higher the beam rises.

Thus, if the beam starts to rise from the middle of a line, it will rise:

- Higher by 1/2 pixel than if the beam had gone up from position C0=0.
- Lower by 1/2 pixel than if the beam had risen from position C0=63.

One idea (not that far-fetched, Cheshirecat would say) is to trigger the 2nd HSYNC-VSYNC on each of the 64 screen positions to achieve 1/64th pixel positioning accuracy



This diagram shows the positioning of the beam at the vertical level of a pixel when it has arrived at the top of the screen, starting from a VSYNC activated on the different positions of C0 of a line.

The CTM is accurate enough to handle that. CPC magic! Boo to the C64 and Amiga!

The human eye, however, is not able to see movement at this level of precision. Thus, the CPC on a CTM monitor can manage fluid vertical scrolling at 1/64th of a pixel (and all lower variations).

This is demonstrated in SHAKER from version 2.1.

15.4 THE RIGHT MOMENT...

If R7 is updated without "precautions", a new VSYNC may occur during or after the current frame. In this situation, the monitor must handle multiple VSYNC or the absence of VSYNC after the update, and this results in frame breaks.

The monitor is simply trying to set its image to the new position of C4=R7. This operation can take place faster or slower depending on the "v-hold" setting of the monitor.

It is possible to avoid this synchronization stall of the monitor by acting so that C4 returns to the new value of R7 in the same place as the old value of C4=R7. This requires modifying R4 so that it goes back to 0 earlier if the new C4=R7 to be reached is higher than the old one, or conversely to enlarge R4 so that C4 goes back to 0 later if the new C4=R7 to be reached is lower than the old one. Just imagine that it is the counters which end up where they should be.

This little gymnastics of repositioning the counters prevents the monitor from losing the VSYNC, which can be annoying for a program that cannot suffer this type of visual artifact.

Otherwise, if your code has time, it is always possible to hide this stall by acting on R1 and / or R6, or even by putting all the black inks a "certain time", but there are some perverts who titillate the V-Hold of their monitor in order to track down the deviant's insubordinate of the diktat of fundamentalist purists.

16 SYNCHRONIZATION : REGISTER R2

16.1 GENERAL

The CRTC R2 register defines when **HSYNC** occurs.

HSYNC occurs in relation to the position of the **COvs** character (in the CRTC sense). During **HSYNC**, in principle, nothing is displayed anymore.

The length in μsec of the **HSYNC-CRTC** is fixed with the 4 less significant bits of the R3 register. See Chapter 14.1, page 114.

The timing of **HSYNC** is different for different CRTC's and is not based on the beginning of a CRTC character. See Chapter 14.4, page 116.

The display of pixels does not start (and does not stop) on a word boundary, see byte (depending on conditions) for HSYNC. See Chapter 14.8, page 123.

The GATE ARRAY is faster to manage HSYNC than to display characters read by CRTC's 0, 1 and 2. The HSYNC starts earlier and is "visible" on the character preceding the one pointed by R2, which has not yet been displayed.

THE ASIC's (CRTC's 3 and 4) manage a HSYNC consistent with the C0 value displayed, delaying the display of the HSYNC by 1 μsec .

Examples :

- If R2 is 10, on a CPC with CRTC (0, 1 and 2) then HSYNC starts from C0 displayed=9 (R2-1) over a length of R3 μsec .
- If R2 is 10, on a CPC with "CRTC" (3 and 4) then HSYNC starts from C0 displayed=10 over a length R3 μsec .

Because of this discrepancy, the calibration of a CM14 monitor (464+/6128+) is different from that of a CTM 640/644 (464/664/6128).

However, CRTC 4 does not come with a CM14, but it behaves like a CPC+ at the HSYNC signal. Plugged into a CTM 640/644, the image is shifted to the left because HSYNC occurs 1 μsec later. In order to ensure visual compatibility with other CRTC's, this can be overcome by programming R2 with a value 1 lower than that programmed for other CRTC's.

Conversely, plugging a CRTC 0, 1, or 2 CPC into a CM14 monitor should cause a shift to the right of the image.

On a CTM monitor, the first character visible on the left is the 15th character from the C0=R2 position if $R3 > 5$. (If R2=49 (with R0=63), the 1st visible character is C0=63).

This difference between consideration and display does not change the CRTC's counter management behaviour when R2 and R3 are modified.

As we have seen, the GATE ARRAY is slower to display characters than to take into consideration the HSYNC signal, but there is **also a delay between the instruction of the Z80A that updates the CRTC and the speed of the latter to consider.**

Thus, if R2 is modified very precisely on the character (CRTC) concerned, the CRTC receives the information slightly later, reflecting here the internal delays specific to the Z80A OUT instruction. This slightly reduces the size of the "displayed" HSYNC. See Chapter 14.2, page 115.

The CRTC has a period during which it "agrees" to consider R2.

The GATE ARRAY in this situation, receives the HSYNC signal slightly later, which has an impact on the "**displayed**" length of the HSYNC.

HSYNC treatment begins with HSYNC-GA treatment, which lasts a maximum of 6 μ sec. It is on the HSYNC-GA that the monitor synchronizes for each line.

If this HSYNC changes position or length (and if this length exceeds 2 μ sec) several times during scanning it causes distortion of the image by the monitor.

During the first 2 μ sec the GATE ARRAY does not send a synchronization signal (H/Csync) to the monitor. HSYNC-GA is dependent on HSYNC-CRTC (start and length):

- It begins at the same time as the CRTC's HSYNC.
- It stops at the same time if the CRTC's HSYNC lasts less than 6 μ sec.

A 2 μ sec HSYNC does not cause a synchronization signal to be sent to the monitor. Above this duration of 2 μ sec, the monitor will try to synchronize the displayed line.

Distortion effects may appear:

- If the HSYNC is too short ($>2 \mu$ sec and $< 6 \mu$ sec).
- If multiple HSYNC of length $> 2 \mu$ sec are generated on the same line.
- If the HSYNC(s) are not vertically aligned.

During an HSYNC, the different CRTC's no longer manage the $C0=R2$ condition, which prevents a HSYNC from restarting within an HSYNC.

CRTC 2 is the champion in the difference in management of certain conditions occurring on specific C0 values during an HSYNC:

- This is the case when $C0=0$ and $C4=R7$ to generate a VSYNC. If a HSYNC takes place during this period, then VSYNC is considered enabled.
- This is the case when $C0=0$ for the BORDER to be disabled. A HSYNC placed on the zone or $C0=0$ does not allow to disable the BORDER until the next $C0=0$.
- An effective last line condition during HSYNC forces C4 to increment instead of being zeroed.

16.2 HSYNC WHEN R2 IS PREDEFINED

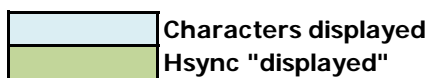
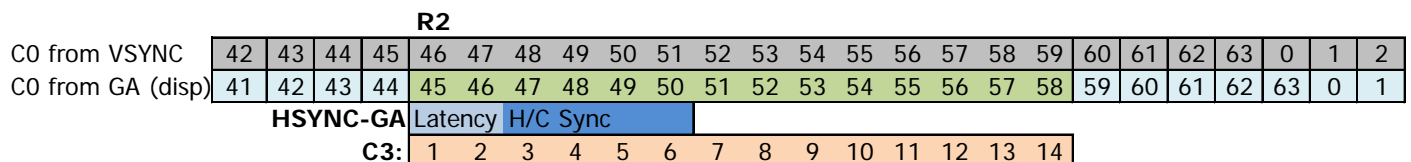
The following diagrams show the generation of HSYNC, as it occurs when R2 was programmed before C0vs=R2, which is in principle the general case.

The characters are indicated according to the two timelines, since the HSYNC is managed without "delay" by the GATE ARRAY.

CRTC 0, 1, 2

CRTC-R2=46

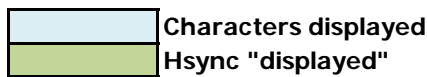
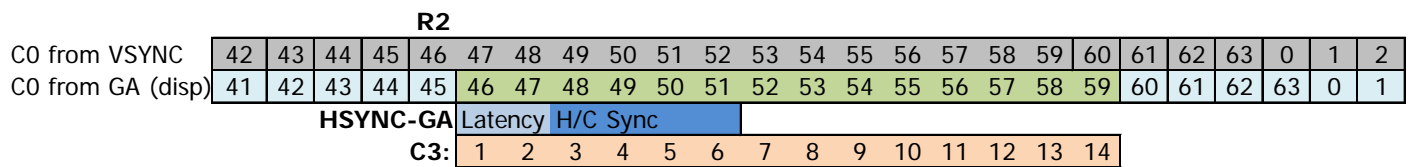
CRTC-R3=14



CRTC 3, 4

CRTC-R2=46

CRTC-R3=14



16.3 UPDATING R2 DURING HSYNC

During the processing of HSYNC CRTC, an update to R2 is no longer considered if the purpose of this change is to start a new HSYNC during HSYNC.

Note :

- This lack of consideration avoids a crash of the circuit, which would only generate HSYNC in the situation or R0 would be less than R3. This is particularly the case when R0 is less than R3, which implies that C0 can pass several times on the same value (equal to R2).
- On CRTC 0, two HSYNC's cannot be contiguous, while there is a management bug on the other CRTC's in this case (they misjudge C3=R3).

INFINITE HSYNC :

The R2 management bug on CRTC's 1, 2, 3 and 4 allow for the creation of an infinite HSYNC (and beyond).

If, for example, we place $R0 = 0$, $R2 = 0$ and $R3 = 1$, we will ask the CRTC to generate a **HSYNC** of 1 μ Sec at the position $C0 = R2 = 0$ and ask it to make a HSYNC for all the μ sec.

On the 2nd character, C0 is still equal to R2.

On a CRTC 0, the **HSYNC** will not take place. It will occur on the 3rd $C0 = 0$.

On the other CRTC's, the **HSYNC** does not end and C3 will overflow. C3 will increment up to 15, return to 0 and then back to 1.

At the end of the overflow of C3, if C0 is still equal to R2 (= 0), then the HSYNC will again continue its route, and C3 overflow again, and so on.

The differences in the consideration of R2 according to the CRTC's are detailed on the diagrams below and describe the update of R2 on different values of COVS during the **HSYNC**, and its impact.

CRTC 1, 2

CRTC-R2=11

CRTC-R3=10 (HBL Size=10 chars)

		R2																																							
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		Hsync-GA: Latency H/C Sync																																							
		C3:																																							
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 17										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:																																							
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 18										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:																																							
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 19										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:																																							
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 20										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:																																							
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 21										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:										11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10										(overflow de C3)																			
		1 2 3 4 5 6 7 8 9 10																																							
		R2										OUT CRTC-R2, 22										R2																			
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39	40				
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38	39				
		C3:										1 2 3 4 5 6 7 8 9 10										C3: 1 2 3 4 5 6 7 8 9 10																			
		1 2 3 4 5 6 7 8 9 10																																							

Characters displayed
 Hsync "displayed"

CRTC 3, 4

CRTC-R2=11

CRTC-R3=10 (HBL Size=10 chars)

	R2																																		
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	Hsync-GA: Latency H/C Sync																																		
	C3: 1 2 3 4 5 6 7 8 9 10																																		

		R2										OUT CRTC-R2, 17	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10																																		

		R2										OUT CRTC-R2, 18	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10																																		

		R2										OUT CRTC-R2, 19	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10																																		

		R2										OUT CRTC-R2, 20	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10																																		

		R2										OUT CRTC-R2, 21	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10										C3: 11 12 13 14 15 0 1 2 3 4 5 6 7 8 9 10																								

		R2										OUT CRTC-R2, 22	R2																						
C0 from VSYNC	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37	38
C0 from GA Disp	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	37
	C3: 1 2 3 4 5 6 7 8 9 10										C3: 1 2 3 4 5 6 7 8 9 10																								

	Characters displayed
	Hsync "displayed"

16.4 VSYNC CONSIDERATION DURING HSYNC

16.4.1 GENERAL

The assessment of the VSYNC condition is carried out on either C0 for CRTC's 0, 1 and 2, but **only when C0=0 for CRTC's 3 and 4.**

In any case, C4 must be equal to R7, either because C4 gets there or because R7 has been programmed with the value of C4. This is also true when C4 reaches R7 from additional line management.

For all CRTC's except the CRTC 2, there is no problem with a **VSYNC** condition occurring during HSYNC. See the following paragraph for details on CRTC 2.

The value of R2 has been applied to a full frame in the following schemas and describes HSYNC's of different lengths that encroach on the VSYNC test area.

The part of the line on the diagrams is the one that corresponds to C4=R7-1 (or previous if R7 is 0), C9=7 (when R9=7).

16.4.2 CRTC 0, 1

		R2												Vsync					
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=12	C3:	1	2	3	4	5	6	7	8	9	10	11	12						

		R2													Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=13	C3:	1	2	3	4	5	6	7	8	9	10	11	12	13					

		R2													Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=14	C3:	1	2	3	4	5	6	7	8	9	10	11	12	13	14				

		R2														Vsync			
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=15	C3:	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15			

16.4.3 CRTC 3, 4

	R2													Vsync					
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=12	C3: 1 2 3 4 5 6 7 8 9 10 11 12																		

	R2													Vsync					
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=13	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13																		

	R2													Vsync					
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=14	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13 14																		

	R2													Vsync					
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=15	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15																		

16.4.4 CRTC 2

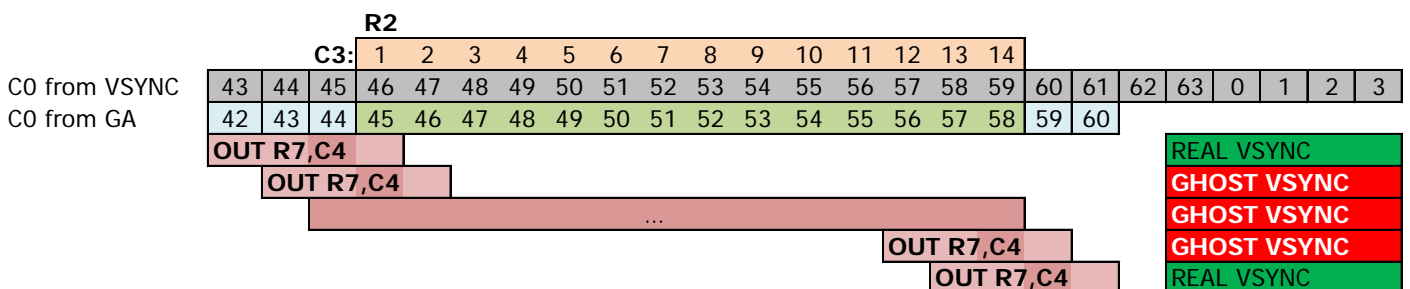
The VSYNC condition (C4=R7) is evaluated as soon as C0=R0 on the last line before C4 is equal to R7. It is also evaluated for all C0 values during which C4=R7. If this first evaluation takes place when the HSYNC is in progress (when the value of C0 or the condition occurs is between R2 and R2+R3-1), then a GHOST VSYNC starts.

Indeed, if the VSYNC condition were only "ignored" during HSYNC, it would occur immediately when leaving HSYNC, since the C4=R7 condition is still true, and the evaluation takes place on all values of C9 and C0.

There is certainly a nice conflict on the activation of the VSYNC pin (pin 40) when the HSYNC pin (pin 39) is in the high state.

VSYNC can no longer occur because the CRTC has enabled its HSYNC counter and will therefore only be able to accept a new VSYNC condition when GHOST VSYNC is completed.

The following diagram precisely describes the inhibition of VSYNC when R7 is modified with the current C4.



The following diagrams describe the different values of C0 on which the VSYNC condition is evaluated according to the value of R2 and R3.

	R2														Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=12	C3: 1 2 3 4 5 6 7 8 9 10 11 12																		

	R2														Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=13	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13																		

	R2														No Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=14	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13 14																		

	R2														No Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2
R3=15	C3: 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15																		

It is possible to circumvent CRTIC 2's limitation to treat its VSYNC in several ways if you want to position R2 and R3 freely.

One solution is to manage R7 yourself, so that the VSYNC cannot be processed during HSYNC, and position R7 with C4 once the HSYNC is finished.

The FAKE VSYNC mentioned in chapter 7.3 does not work properly on all the CPC's I have been able to test. It is therefore a solution to avoid while we don't know what this difference is related to and whether it can be overcome. From my observations, it is not the update of bit 0 with 1 of the PPI's port B that generates a VSYNC, but rather the precise moment when the CRTIC cancels the GHOST VSYNC.

Another solution is to change the size of the HSYNC at the right time, but there is a subtlety. The following result is therefore presented subject to caution, because I have not yet understood why VSYNC is not generated when R3 goes from 15 to 12, while it is for R3 which goes from 14 to 12 :

The value of R3 is reduced at the time the VSYNC condition is to be evaluated.
In this situation :

- If R3 goes from 14 to 12 during HSYNC, VSYNC occurs.
- If R3 goes from 15 to 12 during HSYNC, VSYNC does not occur.

	R2														OUT R3, 12		Vsync			
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3	
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	
R3 init=14	C3: 1 2 3 4 5 6 7 8 9 10 11 12														13	14				

	R2														OUT R3, 12		No Vsync				
C0 from VSYNC	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2	3		
C0 from GA	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63	0	1	2		
R3 init=15	C3: 1 2 3 4 5 6 7 8 9 10 11 12														13	14	15				

16.5 BORDER AND HSYNC

16.5.1 CRTIC 0, 1, 3, 4

The management of background or BORDER display, with conditions $C0=0$ and $C0=R1$, is considered for all CRTIC's except 2.

16.5.2 CRTIC 2

The condition for restoring the background display occurs when $C0=0$ (and $C4$ has never reached $R6$).

BORDER is enabled when $C0=R1$.

However, during HSYNC, this $C0=0$ test is not performed.

(to see if it is the same with $C0=R1$ to activate the BORDER)

In this condition, **BORDER is not disabled**.

That is BORDERLINE, we can say!

16.6 THE RIGHT MOMENT...

If $R2$ is updated without "precautions", a new HSYNC may occur during or after the end of the current line. In this situation, the monitor must handle multiple HSYNC's or the absence of HSYNC after the update, and this results in horizontal distortion of the image.

The monitor tries to set its image to the new position of $C0=R2$. Since it takes several lines to achieve this, this results visually in a gradual shift of the lines. This is the same principle as when the length of the HSYNC is changed with a value of less than 6 to shift the image.

Many demos have used these principles ($R2$ and/or $R3$) to perform horizontal image distortions or scrolling.

As for $R7$ at the vertical level, it is possible to avoid this horizontal synchronization stall of the monitor by acting so that $C0$ returns to the new value of $R2$ in the same place as the old value of $C0=R2$. This requires modifying $R0$ so that it goes back to 0 earlier if the new $C0=R2$ to be reached is higher than the old one, or conversely to enlarge $R0$ so that $C0$ goes back to 0 later if the new $C0=R2$ to be reached is lower than the old one. You just have to imagine that it is the counters that come to place where they should be.

These little gymnastics of repositioning the counters prevent the monitor from losing the HSYNC (or having two in less than 64 μsec), which can be annoying for a program which cannot suffer this type of visual artifact.

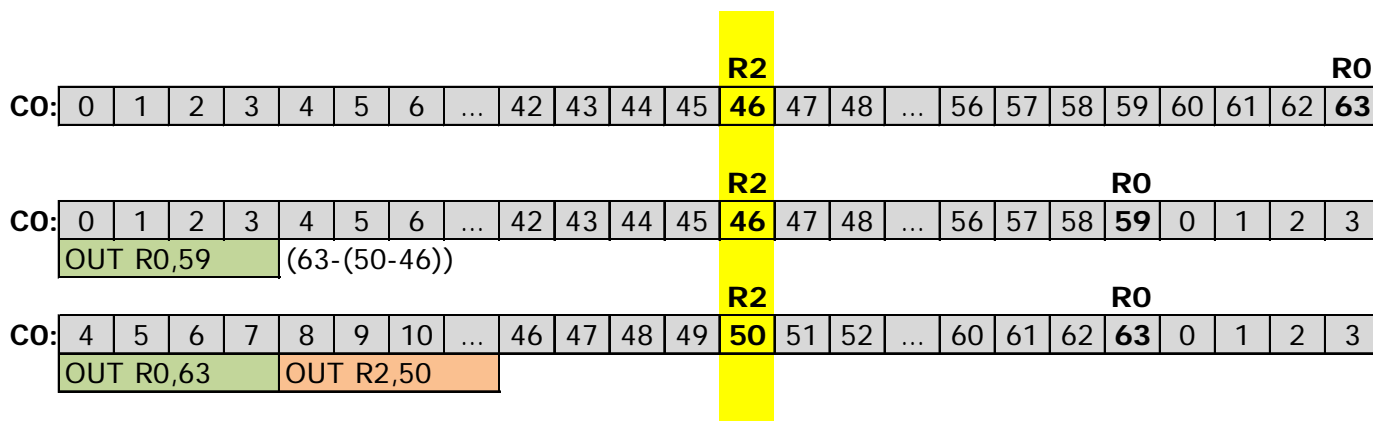
Otherwise, if the CPC is not intended to serve the video broadcasting diktat of the organizers of large competition meetings (to which the diktat mentioned in Chapter 15.4 is subject) or adapt to pretty LCD flat screens, it is always possible to hide this stall by modifying $R2$ in an area not displayed (for example during the VSYNC).

It is also possible, as per vertical synchronisation, to act on $R1$ and / or $R6$, or even set all the inks to black at a "specific time".

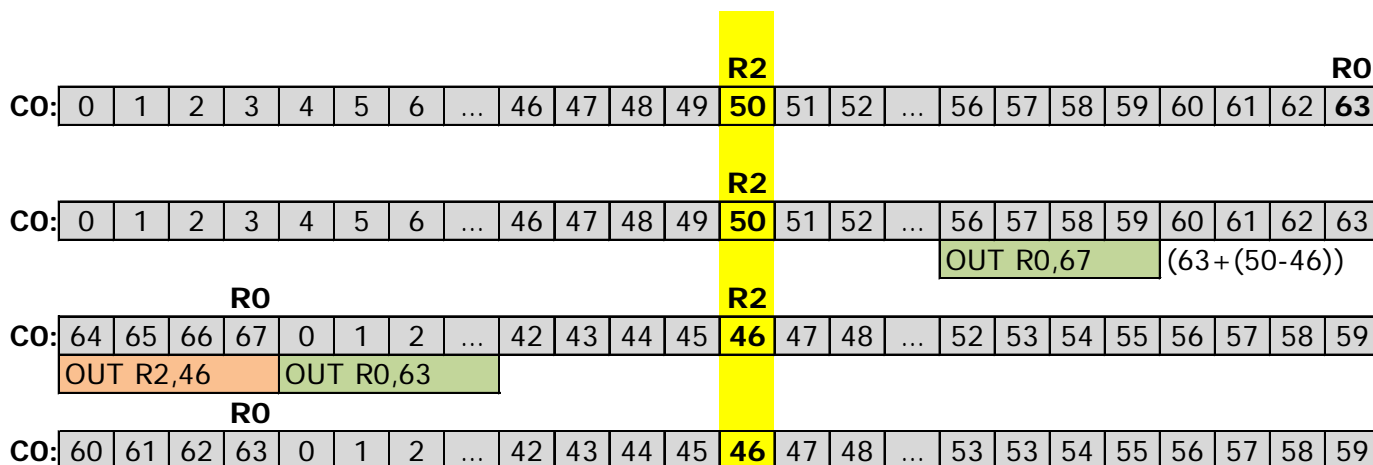
Setting the H-Hold potentiometer, however, requires a small flat screwdriver to be set to a CTM monitor.

Here are nevertheless 2 diagrams to translate the gymnastics of the counters necessary to go from R2 from 46 to 50 and vice versa, from 50 to 46 (the choice of these values being neither fortuitous nor independent of my will) without traumatizing the screen.

16.6.1 Go from R2=46 to R2=50 on 64 μsec lines.



16.6.2 GO from R2=50 to R2=46 on lines of 64 μsec



17 DISPLAY : REGISTER R1

17.1 GENERAL

The function of this register is to define the number of horizontal characters displayed on a line. Its value is expressed by the number of CRTIC characters (as a reminder, each CRTIC character occupies 2 bytes in RAM).

It also plays an important role in memorizing the current video pointer.

In general, the CRTIC generates $R0+1$ characters on a line, of which $R1$ characters will be displayed. When $R1$ Characters are displayed (DISPLAY ENABLE ON) then the display is inhibited, and the "Border" is displayed on CPC (DISPLAY ENABLE OFF) via the GATE ARRAY.

Note that the DISPLAY ENABLE Pins have various names, and we can find it under other exotic names such as DISPTMG or DE, depending on the different CRTIC documentation.

To display all of the characters that the CRTIC can generate for a line, $R1$ should in principle be $R0+1$. Indeed, the DISPLAY ENABLE "Flag" is set to OFF to generate border when $C0=R1$.

However, $C0$ can never exceed $R0$.

To display all programmed characters with $R0$, it is possible to prevent $C0$ from reaching $R1$, either by positioning $R1 > R0$, or by changing the value of $R1$ during the line.

In this situation, a problem arises because the equality between $C0$ and $R1$ is used to update the video pointer when $C9=R9$ (last line of a "character").

This defect in updating therefore causes a repetition of the character lines, under conditions specific to each CRTIC.

Note :

This problem, caused by the dynamic counter management is a defect because it does not allow the video counter to reach 128 bytes for 1 line (64 μ sec), which can lead some unfortunate people to use 65 μ sec screens by line by programming $R0$ at 64 with a single horizontal synchronization position for these 65 μ Sec lines ...

This allows for the addition of a hiss to the music played in the demos and to verify that the monitor is poorly adjusted.

Without artifice this does not allow the possibility of getting a video pointer where the more significant address byte does not vary during the display of a line. This "trick" saves CPU when it comes to displaying data, because you just increment an 8-bit register instead of 16-bit for the video pointer. Which is why, unfortunately, so many screens are formatted with lines 64 bytes wide in "minimized screen", 16 less than the standard width.

When $C0$ goes back to 0 (following a condition $C0=R0$) then the display is authorized (DISPLAY ENABLE ON). Note that if $C0$ returns to 0 because it reached 255 having overflowed, this does not authorize the display (at least on the CRTIC 0 but is yet to be verified on the other CRTIC's).

Note also that **this condition is not managed by the CRTIC 2 during the HSYNC.**

If $R1$ is zeroed then no more characters are displayed, regardless of the CRTIC of a CPC.

The border begins on position $C0=R1$ (considering, for CRTC 0, that the SKEW DISP function is not used).

Note :

This is not the case on the BBC with the Hitachi HD6845SP (type 0) either with Samsung KS68C45S or a VLSI VL68C45S23PC. (But why am I talking about this in a document dedicated to the CPC, me?). (Why not the PD7220 NEC as long as I'm here?)

In the diagrams below, and in some introductory words, I refer to two memory pointers in the CRTC, which I named **VMA** and **VMA'**.

When the CRTC displays characters, it always uses **VMA** pointer.

This pointer is incremented each time a character is treated by the CRTC, whether displayed or not. In some "pre-release" versions of the CRTC, this pointer was not managed during the VSYNC, but that does not concern the CRTC's of the CPCs to my knowledge.

When $C0=R1$ and $C9=R9$, then the **VMA** current pointer is transferred to the **VMA'** pointer.

When $C0=0$, at the start of the line, the **VMA'** line pointer is transferred to the **VMA** current pointer, except for the first character ($C4=0$).

17.2 DISPLAYS ACCORDING TO R1

17.2.1 DISPLAY WITH R1 <= R0

The following diagram describes R1 management in "standard" programming of the CRTC on a CPC which has just been switched on with a standard ROM BASIC.

Initial data: CRTC-R0=63 / **CRTC-R1=40** / **CRTC-R9=7** / CRTC-R12=0 / CRTC-R13=0

C0=0	C0=R1 & C9=R9	VRAM-C9-Bit 0..2	C0:	0	1	2	3	...	37	38	39	40	41	42	43	44	45	...	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	0	0	1	2	3	...	37	38	39	DISP-OFF	BORDER						
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	1	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	2	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	3	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	4	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	5	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	6	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 :	7	0	1	2	3	...	37	38	39	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	0	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	1	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	2	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	3	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	4	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	5	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 :	6	40	41	42	43	...	77	78	79	DISP-OFF							
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 :	7	40	41	42	43	...	77	78	79	DISP-OFF							

17.2.2 DISPLAY WITH R1 > R0

The following diagram describes the display when R1 is programmed with a value greater than 63.

Initial data: CRTC-R0=63 / CRTC-R1=64 / CRTC-R9=7 / CRTC-R12=0 / CRTC-R13=0

C0=0		C0=R1 & C9=R9	VRAM-C9-Bit 0..2	C0:	R0 R1															
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 0	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 1	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 2	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 3	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 4	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 5	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 6	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 7	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 0	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 1	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 2	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 3	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 4	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 5	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 6	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'			CRTC-VMA C9: 7	0	0	1	2	3	...	53	54	55	56	57	58	59	60	61	62	63

If R1 > R0, then C0 is never equal to R1 (when C9=R9), and VMA' is therefore not updated with VMA.

This causes a character repetition because the current address is not updated during the change of one "line-character" (when C9=R9).

Note 1 :

Only the first 10 bits are not updated in this context.

The bits that determine the block number (Character line) (C9 or C5) continue to "participate" in the address. See Chapter 20, page 199.

Note 2 :

Insofar as the conditions allow the address update, modifying R12/R13 allows for this repetition to be avoided. In practice, this allows you to put the "lines" when C0 returns to 0 several times during a "line". However, CRTC's 0 and 2 generate a border byte, knowing that CRTC 0 can still prevent the generation of this byte by consuming CPU. See Chapter 19.2, page 162.

Note 3 :

According to the CRTC, the initial update of CRTC-VMA'/CRTC-VMA via R12/R13 is not the same.
See Chapter 19.2, page 162.

17.3 DYNAMIC R1 UPDATE

The condition C0=R1 is considered immediately on a line.
It can occur several times on the same line if R1 is reprogrammed.

When the first condition C0=R1 is true, there is no longer any display of characters, and the BORDER is displayed.

However, even if only the BORDER is displayed, the **VMA pointer continues to count** (the CRTC being only a large field of flowering counters,...).

If R1 is updated again during the line to meet the condition C0=R1 when C9=R9 then **this will cause an update of the video pointer**.

In other words, the modification of R1 during the BORDER R1 display allows for the video pointer to be updated **without the data being displayed**.

The diagrams below show these behaviours when C4 > 0.

CO=0	CO=R1 & C9=R9	VRAM-C9-Bit 0..2	UpdCO:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31					
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=26	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	DISP-OFF										
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1	R1=25	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	DISP-OFF											
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2	R1=24	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	DISP-OFF												
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3	R1=23	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	DISP-OFF													
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4	R1=22	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	DISP-OFF														
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5	R1=21	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	DISP-OFF															
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6	R1=20	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	DISP-OFF																
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7	R1=19	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	DISP-OFF																	
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	36	DISP-OFF																		
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1	R1=17	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	35	DISP-OFF																			
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2	R1=16	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34	DISP-OFF																				
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3	R1=15	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	DISP-OFF																					
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4	R1=14	19	20	21	22	23	24	25	26	27	28	29	30	31	32	DISP-OFF																						
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5	R1=13	19	20	21	22	23	24	25	26	27	28	29	30	31	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6	R1=12	19	20	21	22	23	24	25	26	27	28	29	30	DISP-OFF																								
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7	R1=11	19	20	21	22	23	24	25	26	27	28	29	DISP-OFF																									
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=12	30	31	32	33	34	35	36	37	38	39	40	41	DISP-OFF																								

CO=0	CO=R1 & C9=R9	VRAM-C9-Bit 0..2	UpdCO:	0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=64	0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		0	1	2	3	...	37	38	39	40	41	42	43	44	45	46	47	48	49	50	51	52	53	54	55	56	57	58	59	60	61	62	63
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7	R1=40	0	1	2	3	...	37	38	39	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		40	41	42	43	...	77	78	79	DISP-OFF																							
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7		40	41	42	43	...	77	78	79	DISP-OFF																							

CO=0	CO=R1 & C9=R9	VRAM-C9-Bit 0..2	UpdCO:	R1	R0
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=40	0 1 2 3 ... 37 38 39	40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 7	R1=64	0 1 2 3 ... 37 38 39	40 41 42 43 44 45 46 47 48 49 50 51 52 53 54 55 56 57 58 59 60 61 62 63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		0 1 2 3 ... 37 38 39	DISP-OFF
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7		0 1 2 3 ... 37 38 39	DISP-OFF

CO=0	CO=R1 & C9=R9	VRAM-C9-Bit 0..2	UpdCO:	R1	R0
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0	R1=40	0 1 2 ... 32 33 34 35	36 37 38 39 40 41 42 43 44 45 ... 51 52 53 54 55 56 57 58 59 60 61 62 63
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7		0 1 2 ... 32 33 34 35	36 37 38 39 DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7		DISP-OFF	CRTC-VMA +++++
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 0		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 1		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 2		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 3		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 4		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 5		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'		CRTC-VMA C9 : 6		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF
CRTC-VMA=CRTC-VMA'	CRTC-VMA'=CRTC-VMA	CRTC-VMA C9 : 7		80 81 82 ... 112 113 114 ##	## ## ## ## DISP-OFF

17.4 VMA'/VMA WHEN C4=0

There are differences between CRTC's for the assignment of the video pointer with the values programmed in R12 and/or R13 when C4=0 and C0=0.

17.4.1 CRTC 0, 3, 4

The first line character begins with the address defined by R12/R13, whatever the value of R1. On the first line of the first character of a "screen" (C4=C9=C0=0), **the VMA' pointer is updated using the content of R12/R13.**

This update is followed by the **VMA pointer update with VMA'.**

If $R1 > R0$, the VMA' pointer is no longer updated, and the lines are repeated.

In this circumstance, when a new screen begins, **VMA' is updated and all the lines displayed become identical and equal to pointer R12/R13.**

17.4.2 CRTC 1

The first line character begins with the address defined by R12/R13, whatever the value of R1. When you are on the first character of a "screen" (C4=C0=0), **the VMA pointer** (and not VMA' as on CRTC 0) is updated **using the content of R12/R13.**

Note: This update particularity allows for the modification of the offset via R12 and/or R13 on each line (C9 from 0 to R9) of a character while C4=0.

This VMA update, however, has a consequence when $R1 > R0$ throughout the frame.

Indeed, the condition $C0 = R1$ no longer occurs and the **VMA' pointer is no longer updated. VMA' is "frozen" on the last known pointer when C0 reached R1 when C9=R9.**

When C9 = 0, the VMA pointer is reloaded with VMA' when $C4 > 0$.

We have therefore, when $R1 > R0$, a first line character which contains the pointer defined in R12/R13 and on the following, the last pointer updated in VMA'.

The video pointer continues to be increased however, even when BORDER is displayed.

This is true both for the horizontal level (R1 management) and the vertical (R6 management).

The VMA' pointer is 14 bits. When it continues to increment and exceeds the 10-bits definition limit, it can modify the Overscan Bits™ (see Chapter 20.5, page 202) and cause video page changes.

When R1 becomes higher than R0, it should be noted, however, that if the R1 update takes place exactly when $C0=R1$ (R1.JIT), then the condition $C0=R1$ is no longer true and VMA' is not updated. If the modification of R1 occurs when $C0=R1+1$ ($C0 > R1$), then the condition $C0=R1$ is satisfied and VMA' is updated.

Example :

If the display width of a line is 40 characters (&28), the CRTC will be able to display 1024/40 different character lines, i.e. 25 complete lines.

When C4=R6=25, the CRTC stops displaying the character lines, but it nevertheless continues to increment its pointer and to manage the updates of VMA' when C0=R1 & C9=R9.

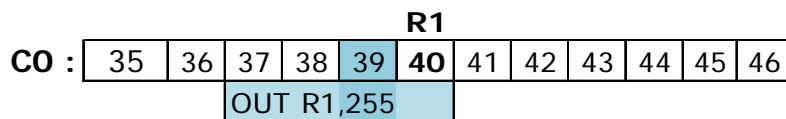
If the modification of R1 (>R0) occurs during this period, the video pointer will have overflowed.

If R1 is modified after C4=24, C9=R9 and C0>R1, then the pointer will be equal to 40 x 25=1000 (the repeated line will contain the characters 1000 to 1023, followed by 0000 to 0015).

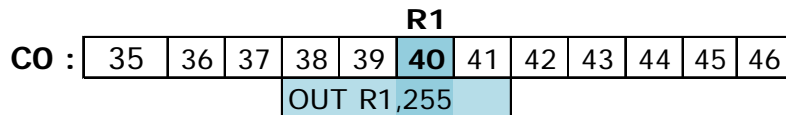
If R1 is modified after C4=25, C9=R9 and C0>R1, then the pointer will be equal to 40 x 26=(1040 and 1023)=16 (the repeated line will contain the characters 0016 to 0055).

VMA' pointer repeated = 960 :

C4=24 / C9=R9
CRTC-VMA'=40x24=960



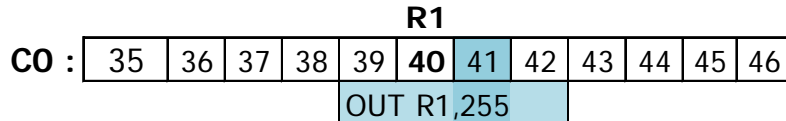
C4=24 / C9=R9
CRTC-VMA'=40x24=960



VMA' pointer repeated = 1000 (40 x 25) :

Condition C0=R1 occurred, pointer VMA' was loaded with VMA.

C4=24 / C9=R9
CRTC-VMA'=40x24=960



17.4.3 CRTC 2

When R1>R0, **neither pointer is updated with R12/R13.**

All lines are identical in this situation.

On the first line, VMA is affected by VMA' (which itself was affected by R12/R13 when C0=R1 on the last screen line).

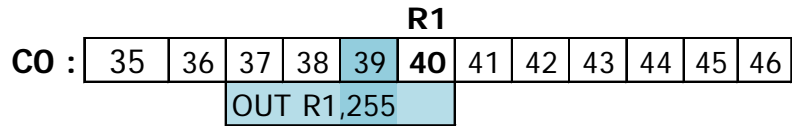
The replicated address follows the same logic as described for CRTC 1.

So, depending on when R1 becomes greater than R0, it's the pointer when the BORDER R1 is handled which is considered.

However, there is a difference with the CRTC 1 when modifying R1 on the exact position of C0=R1. CRTC 1 is faster than CRTC 2 in considering the update of R1 when C0=R1. On CRTC 2, an update of R1 on position C0=R1 arrives too late. VMA' update has already taken place using the old value of R1.

VMA' pointer repeated = 960 :

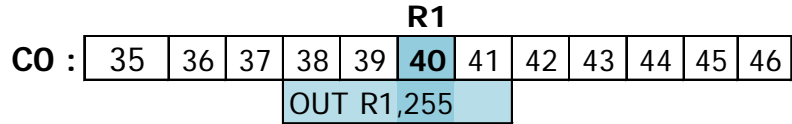
C4=24 / C9=R9
CRTC-VMA'=40x24=960



VMA' pointer repeated = 1000 (40 x 25) :

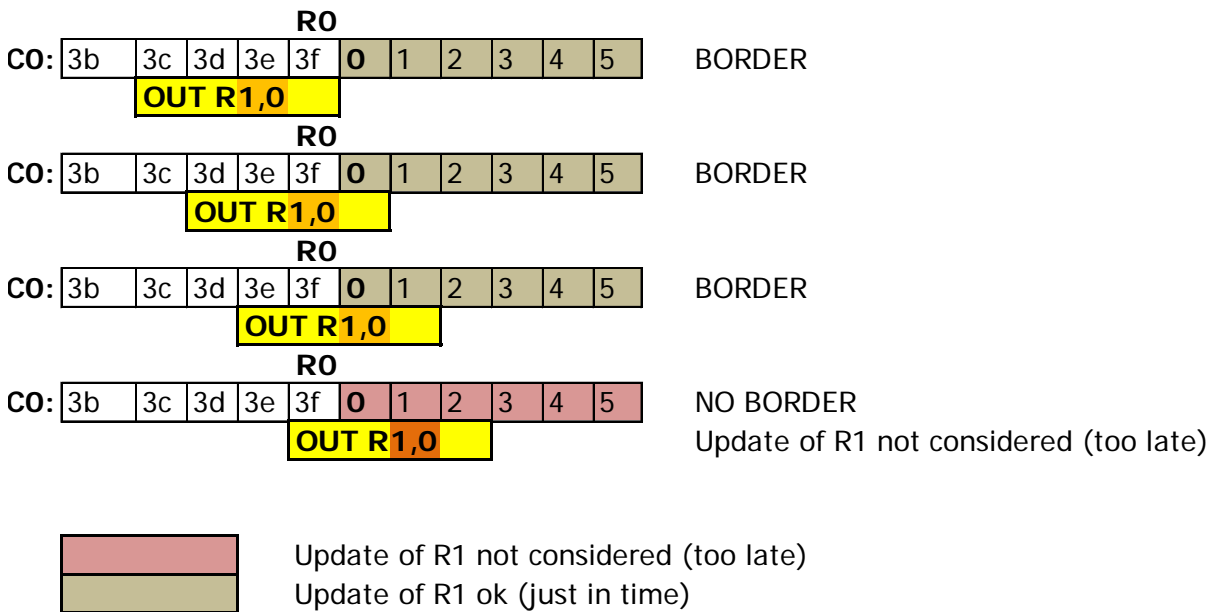
Condition C0=R1 occurred, pointer CRTC-VMA' was loaded with CRTC-VMA.

C4=24 / C9=R9
CRTC-VMA'=40x24=960

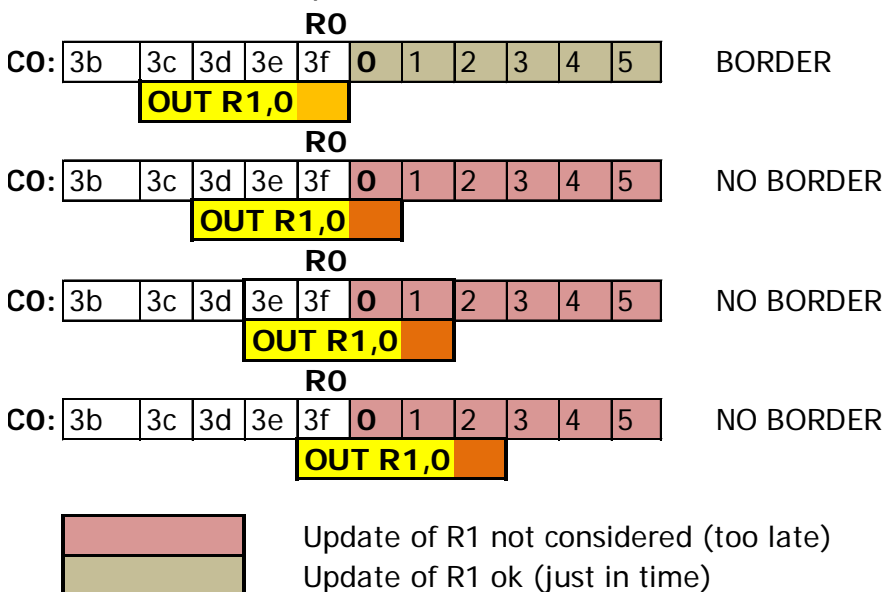


17.5 ACKNOWLEDGMENT R1=0

17.5.1 CRTC 0, 1, 2



17.5.2 CRTC 3, 4



17.6 INTERLINE BORDER

17.6.1 R1=R0 AND C0=R0

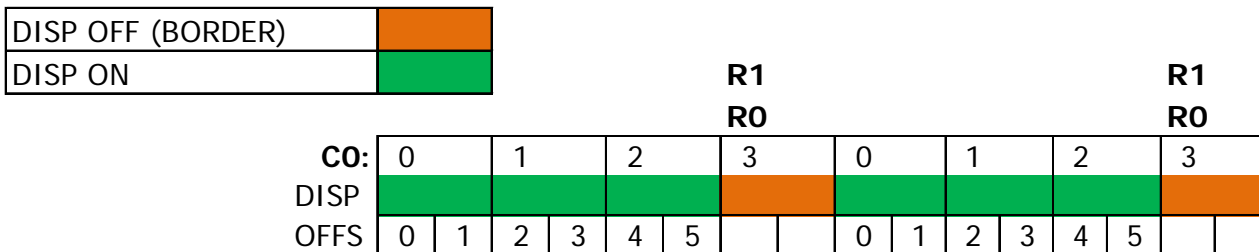
CRTC 0, 1, 2, 3, 4

If R1=R0, all CRTC's will display 1µs of BORDER on the last character (C0=R0).

CRTC-R0=3

CRTC-R1=3

CRTC-R12/R13=0



Note : The pointer in VRAM will continue at offset 6 on the next "character line" (when C9 returns to 0)

17.6.2 R1>R0 AND C0=R0

CRTC 0, 2

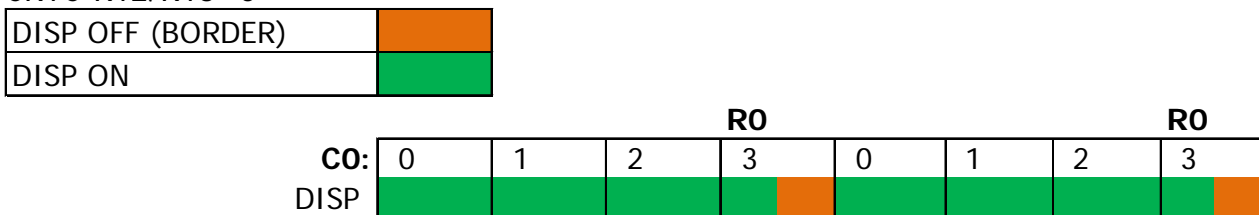
The consideration of the BORDER is anticipated.

1 byte of BORDER is generated (for exactly 0.5 µsec) before C0 goes to 0.

CRTC-R0=3

CRTC-R1=4

CRTC-R12/R13=0



Note 1 : This behaviour remains true whatever the value of R0.

If R0=0, then the display alternates between 1 DISP ON byte, and 1 DISP OFF byte.

When C0 reaches R0 without R1 having been reached, CRTC's 0 and 2 send a "BORDER ON" signal to the GATE ARRAY, which picks it up immediately. These CRTC's are "ahead" of the characters displayed by the GATE ARRAY and send the BORDER signal 0.5 µsec too early. The "BORDER OFF" signal is sent on the character following C0=R0.

Note 2 : The VRAM pointer will get "stuck" on VMA'. If the conditions allow it (according to the CRTC and the counters values), VMA' can be reloaded by updating R12 and/or R13.

Note 3 : The CRTC 0 has a function to generate conditions for later consideration of the BORDER via its R8 register. By playing on the modification of the conditions at the time of their application, it is possible to avoid the generation of this BORDER byte. See Chapter 19.2, page 162.

Note 4 : CRTC 2 does not have the SKEW DISP (R8) function and the BORDER byte cannot be "cancelled" this way. But does LOGON really have to reveal all its secrets?

CRTC 1, 3, 4

CRTC-R0=3

CRTC-R1=4

On these CRTC's, no BORDER bytes are generated between the "screens".

Screens can therefore be created in the displayable area without a byte appearing between the screens. This allows for the possibility of carrying out aggressive plagiarisms...

DISP OFF (BORDER)	
DISP ON	

				R0					R0
CO:	0	1	2	3	0	1	2	3	
DISP									

18 DISPLAY : REGISTER R6

18.1 GENERAL

The function of this register is to set the number of character lines displayed vertically. When this number is reached, the BORDER is displayed.

The BORDER is displayed when $C4=R6$ (1st line-character R6). This rule is true whatever the value of C9.

Except on CRTC 3 and 4, R6 is considered immediately on the current C0.

The DISPLAY ENABLE pin of the CRTC goes to "OFF" when $C4=R6$, in the same way as for the R1 register when $C0=R1$.

In general when the condition is fulfilled to display the BORDER, it is necessary to wait for a new screen ($C4=C9=C0=0$) to restore the displaying of characters.

With register R1, the BORDER is disabled when $C0=0$ and enabled when $C0=R1$.

Whether the border is generated via R1 or R6, the pointer in VRAM continues to be updated. In this case, if the BORDER was activated by the condition on R6, the pointer VMA' continues to be updated.

18.2 BORDER R6 DEADLINES AND PRIORITIES

18.2.1 GENERAL

The state of the DISPLAY ENABLE pin depends on 2 groups of internal CRTC conditions.

As long as the "R6 conditions" are not satisfied, the "R1 conditions" define the state of the DISPLAY ENABLE pin.

When the "R6 conditions" are satisfied, the "R1 conditions" are no longer considered. The common condition for restoring the bottom display is $C4=C9=C0=0$.

In general, the BORDER R6 condition takes precedence over the BORDER R1 condition, however there are some differences between CRTC's.

18.2.2 CRTC 0, 2

Except for the first line of a screen ($C4=C9=0$), positioning R6 with C4 causes the immediate and definitive activation of the BORDER until the next screen.

The condition $C4=R6$ is considered immediately (regardless of the value of C0), and BORDER R6 has priority over BORDER R1.

This is also true during the C4 character(s) generated during a vertical adjustment.

The value $R6=0$ used on the first line ($C4=C9=0$) is treated specifically (see Chapter R6 CONFLICTS) and it is possible, under conditions, to use this conflict to **cancel BORDER R6**. See Chapter 18.3.

18.2.3 CRTC 1

Positioning R6 with C4 causes the immediate activation of the BORDER, which becomes final until the next screen.

The condition $C4=R6$ is considered immediately (regardless of the value of C0), and BORDER R6 has priority over BORDER R1.

As with other registers of this CRTC (for example R3) the value 0 is specifically considered and triggers a BORDER without the condition $C4=R6$ being required.

However, if the condition $C4=R6$ is also fulfilled when $C4=0$, then this BORDER becomes definitive until $C4=C9=C0=0$.

When R6 is set to 0 while $C4 < > 0$, the BORDER is activated while $R6=0$, and it is deactivated as soon as $R6 > 0$ and its new value is different from C4 (in which case, the BORDER R6 is activated for the screen)

18.2.4 CRTC 3, 4

The R6 test is done at the beginning of the line only.

The update of R6 **during the line is therefore not considered.**

If R6 is set to 0 when $C4=0$ but $C0 > 0$, the BORDER is not activated.

The BORDER is activated only when C0 goes to 0 when $C4=R6$.

This is also true during a vertical adjustment.

Note: C4 is not incremented on these 2 CRTC's during vertical adjustment. This implies that if $R6=R4$, then the BORDER will concern this character as well as the vertical adjustment lines defined with R5.

The value of $R6=0$ is not specifically processed and does not temporarily activate the BORDER as on CRTC 1.

18.3 R6 CONFLICTS

18.3.1 GENERAL

In order to correctly manage some conflicts, special processing is often carried out when a register has the value 0 (particularly on CRTC 1, the domain specialist).

This is particularly the case when $R1=0$, because this value creates a potential conflict: deactivation of the BORDER ($C0=0$ following condition $C0=R0$), activation of the BORDER ($C0=R1=0$)

[In this situation, it is the deactivation of the BORDER which is activated]

For R6, the situation is much less well managed, according to the CRTC's.

18.3.2 CRTC 0, 2

Except for the first line of a screen ($C4=C9=0$), positioning R6 with C4 causes the immediate and definitive activation of the BORDER until the next screen.

When $C4=R6=0$ and $C9=0$ on CRTC's 0 and 2, a conflict occurs (this conflict does not exist when $R6>0$).

When R6 is equal to 0 in this situation, the state of DISPLAY ENABLE changes to ON at the beginning of the CRTC character and returns to OFF 0.5 μ sec later.

In other words, on the first line of the screen, there is an alternation of bytes of BORDER and displayable characters (the video pointer continuing to count normally).

At each CRTC character:

- BORDER R6 passes to true because $C4=R6$ and $C9=0$
- BORDER R6 returns to false because for a new screen ($C4=C9=0$)

Note :

This alternation only takes place when the condition R1 is fulfilled (BORDER R1 is false) and the conditions of the conflict exist ($C4=R6=C9=0$).

When the conflict is cancelled (R6 updated with a value > 0), the BORDER does not remain activated as on the other lines (and the other CRTC's).

In this situation however, since R6 has been updated with 0 at least 1 time, the BORDER becomes final when $C0=R1$.

Still in this situation, if we prevent $C0=R1$ on the line $C4=C9=0$ (for example $R1=R0+1$), and R6 is no longer equal to 0, then the BORDER is deactivated on the following line.

In other words, **the condition $C4=R6=0=BORDER$ is cancellable on the first line.**

Note :

Considering for each value of C0 the value of R6 makes it possible to precisely target areas or create this alternation BORDER/CHARACTERS by byte.

By means of a nice line-to-line rupture, this allows you to add nice colours from time to time, via BORDER, to graphic mode 2, for example, which will be called **IIMPSIIA** mode for the most modest, otherwise directly called Mode <write your nickname here>.

Note that it is possible to achieve a BORDER/CHARACTER alternation on CRTC 0 with $R0=0$, but without the counters C4 and C9 being able to count anymore.

18.3.3 CRTC 1

When R6 is updated with 0, the BORDER is activated as long as the register value is 0.

The consideration of each value of C0 of the value of R6 makes it possible to precisely target zones or create this BORDER.

However, if C4=R6=0 (1st line-character of a new screen) during this update, BORDER R6 becomes true first for all the rest of the screen, until the new screen (C4=C9=C0 =0).

18.3.4 CRTC 3, 4

No conflict exists since the management of R6=0 does not exist during the line and is tested only once.

Setting R6 to 0 when C4 and C9 are 0, but C0>0 will have no effect before the new screen (or the BORDER will be activated).

19 DISPLAY : REGISTER R8

19.1 GENERAL

The R8 register contains parameters for the management of the INTERLACE mode for all the CRTC's.

On CRTC's 0, 3 and 4, an additional function exists, which allows for the delaying of the management of activation/deactivation of the BORDER, or to deactivate the display as R6=0 does on CRTC 1 (except C4=0 on CRTC 1).

CRTC	7	6	5	4	3	2	1	0
0	Sc	Sc	Sd	Sd	x	x	i	i
1	x	x	x	x	x	x	i	i
2	x	x	x	x	x	x	i	i
3	x	x	Sd	Sd	x	x	i	i
4	x	x	Sd	Sd	x	x	i	i

Other CRTC	7	6	5	4	3	2	1	0
MC6845*1	Sc	Sc	Sd	Sd	x	x	i	i
UM6845E	UpdM	US	Sc	Sd	Vdrac	Vdrad	i	i

Interlace		
0	0	No interlace
0	1	Interlace Sync Mode
1	0	No interlace
1	1	Interlace Sync & Video Mode

Skew DISPTMG		
0	0	Non Skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

Skew CUDISP		
0	0	Non Skew
0	1	One-character skew
1	0	Two-character skew
1	1	Non-output

19.2 FUNCTIONS « SKEW-DISPTMG »

These functions are only available on CRTCs 0, 3 and 4.

They allow for the activation of the BORDER or to generate a delay on the BORDER R1 management.

Note: If the BORDER ON function is activated, the INTERLACE function on the 2 least significant bits is not considered. (This point requires further investigation).

19.2.1 BORDER ON

This function is activated with **001100xx** on R8.

It allows you to deactivate the display of characters.

The GATE ARRAY generates BORDER in this situation.

The update of the DISPEN signal (DISPLAY OFF) is immediately considered.

The VRAM pointer nevertheless continues to be incremented and the current pointer is updated when $C0=R1$ and $C9=C0=0$.

This function does not affect the BORDER R6 state (when $C4=R6$) and it is therefore possible to switch to one of the 3 other available states.

Note: On CRTC 1, this direct assignment of DISPEN is possible by setting R6 to 0.

However, if $C4=0$, then the condition $C4=R6$ is fulfilled, and this causes the end of display until $C4=C9=C0=0$. This problem does not exist with the BORDER ON function.

19.2.2 BORDER OFF

This function is activated with **000000xx** on R8.

It indicates to stop managing the other "SKEW" functions.

To be tested: Set the 001100xx function, then wait for $C4=R6$ to activate the BORDER, and then set R8 to 000000xx and see if this can cancel a BORDER R6.

19.2.3 BORDER DELAY +1 / +2

These functions are activated with **000100xx** & **001000xx**

They provide a mechanism to delay the BORDER R1 management.

Without this function being activated, we have:

- The BORDER deactivation condition (beginning of line) is performed on the character following $C0=R0$ ($C0=0$).
- The BORDER activation condition (end of line) is performed on character $C0=R1$.

The delay can be 1 or 2 CRTC characters (thus 1 or 2 μ sec) depending on the function used.

The BORDER management conditions **remain the same** as those described above.

However, an acknowledgment counter from C0 is applied according to the function:

When the programmed "delay" is 1 μ sec:

- The BORDER is deactivated on the 2nd character after that or $C0=R0$ ($C0=1$).
- The BORDER is activated on the 1st character after the one where $C0=R1$.
Note: If $R1=R0$, then the BORDER is activated on $C0=0$.

When the programmed "delay" is 2 μ sec:

- The BORDER is deactivated on the 3rd character after that or $C0=R0$ ($C0=2$).
- The BORDER is activated on the 2nd character after the one where $C0=R1$.

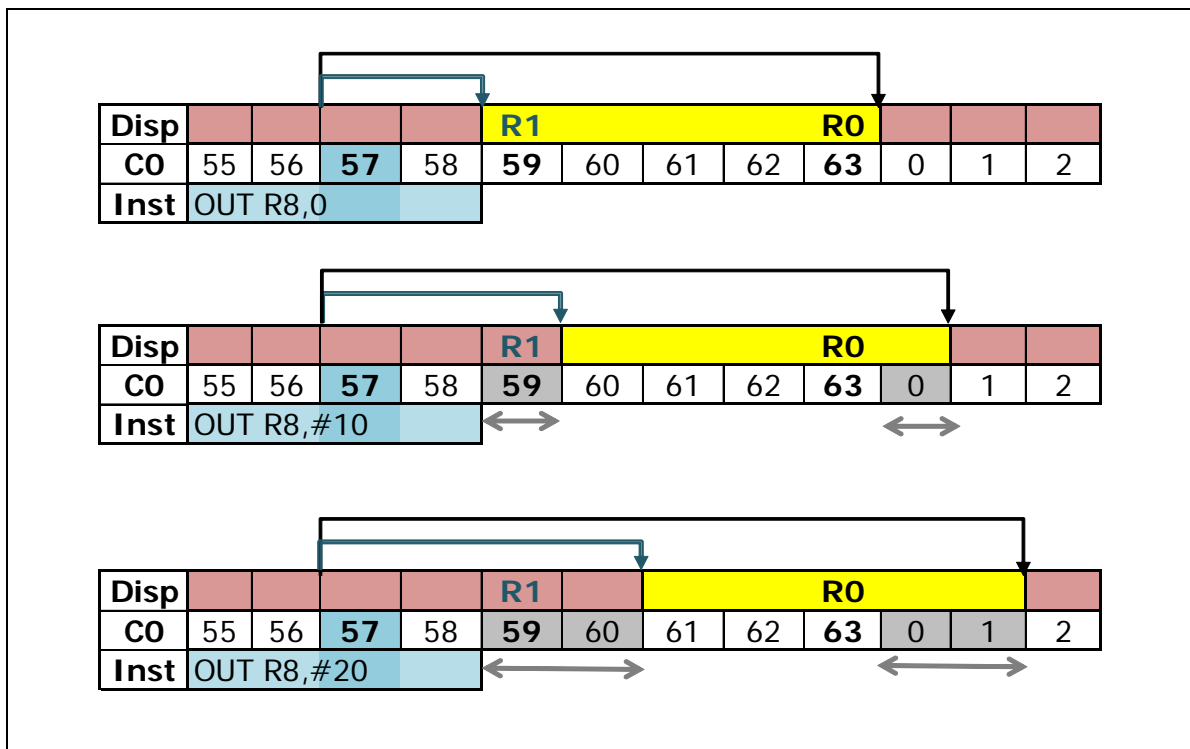
Note: If R1=R0, then the BORDER is activated on C0=1.

The assignment of the video pointer, when C9=R9, follows the same logic when C0 reaches the relative value of C0 with respect to R1.

In other words, the video pointer is stored in relation to the new position of the BORDER.

The consideration of these new test "rules" when R8 is modified is immediate during the line.

The diagram below describes the position of the BORDER according to the programming of the registers, for a standard case. R1=59, R0=63, with a modification of R8 occurring elsewhere than on the corresponding positions of C0.



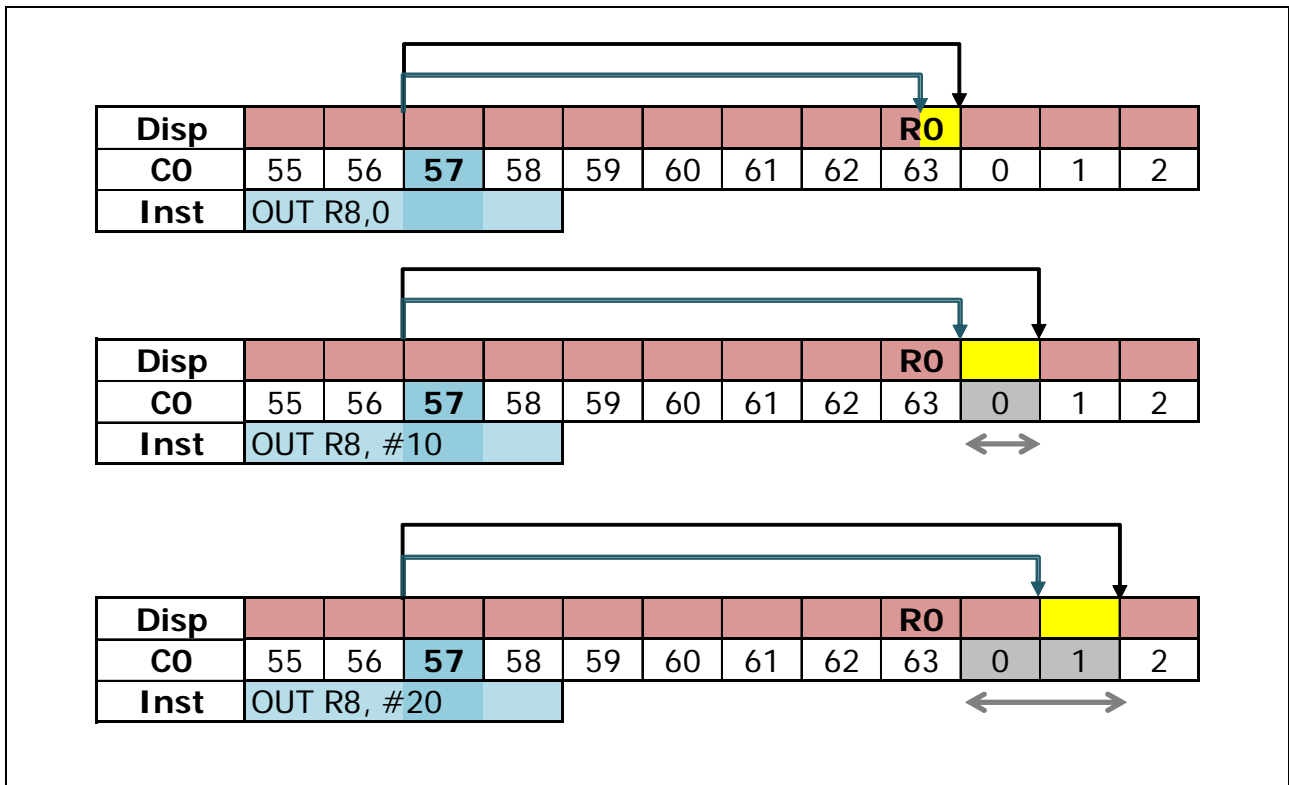
	Character Display
	Border Display
	Gap Skew ↔
→	Border ON on C0=R1 applied
- - - - ->	Border ON on C0=R1 not applied
→	Border OFF on C0=R0 applied
- - - - ->	Border OFF on C0=R1 not applied

19.2.4 NO CONDITION C0=R1

In the chapter devoted to the R1 register (17.2) we saw that on CRTC's 0 and 2, a BORDER byte is generated between "2 lines" when R1 is greater than R0.

The condition C0=R1 not being met during the line, the BORDER signal is then sent 0.5 µsec after the condition C0=R0 is satisfied. The BORDER is disabled on the next character, 0.5 µsec later. The condition C0=R0 therefore replaces the condition C0=R1.

Note: On CRTCs's 1, 3 and 4, in the same context ($R1 > R0$, with for example $R0=63$, $R1=64$), the condition $C0=R1$ is not met, and the CRTC does not send BORDER ON signal to GATE ARRAY. When a delay is programmed using the SKEW DISP functions, the delay is counted based on the transitions of $C0$. In other words, the "deferred" BORDER will be displayed at the beginning of the character, as it would have been on the condition $C0=R1$.



19.2.5 DISINTEGRATION OF THE BORDER ON CRTC 0

There is a period of 1 or 2 μ s, depending on the function used, during which it is possible to "cancel" the 2 conditions. The CRTC 0 has the possibility of removing this byte from BORDER by cancelling the 2 conditions. The CRTC 2 does not have the SKEWDISP functions and therefore cannot use this method to make this BORDER byte disappear between 2 lines.

Note: This method can also be used when $R1 > R0$. The condition $C0=R1$ is just replaced by the condition $C0=R0$ in this case.

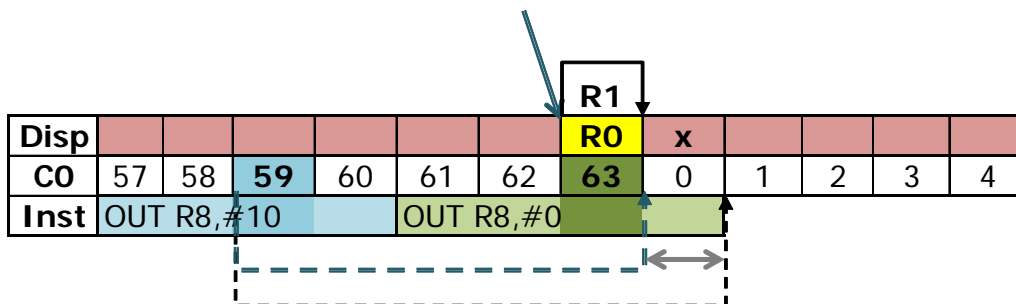
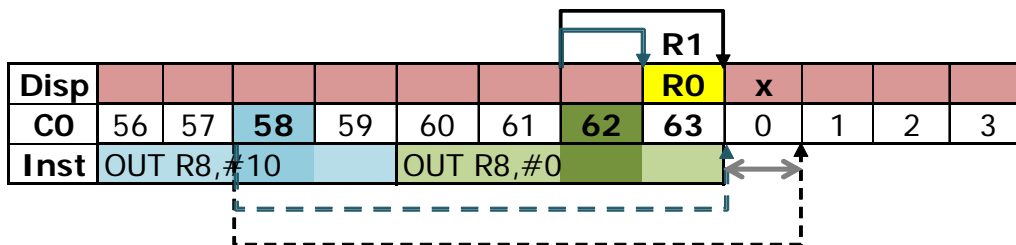
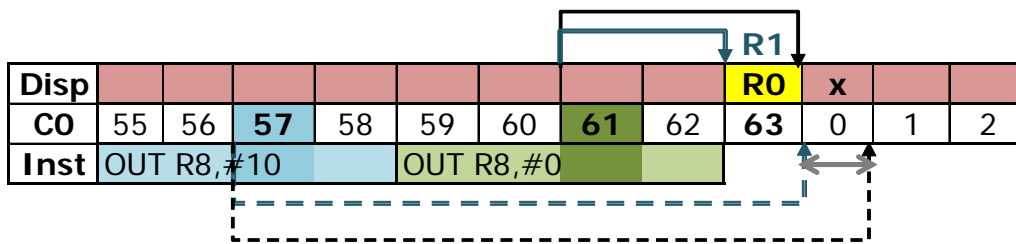
For the different situations presented below, it is considered that:

- $R0=R1=63$.
- The programming of R8 is carried out on several lines. Therefore, the last value programmed on the line is the one present when the 1st OUT is performed on the following line.

19.2.5.1 SKEW DISP+1 is cancelled on $C0 \leq 63$.

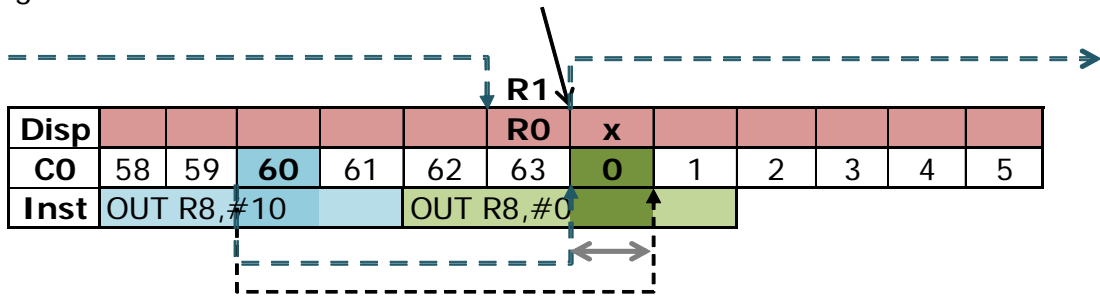
BORDER management is handled with the 2nd OUT.

The programming of the 1st OUT ($R8=\#10$) is ignored



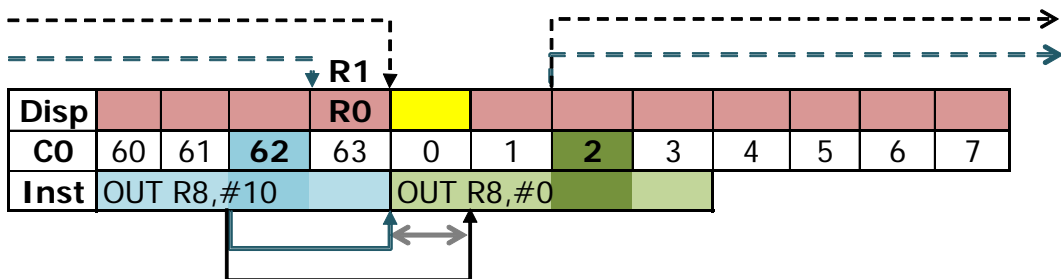
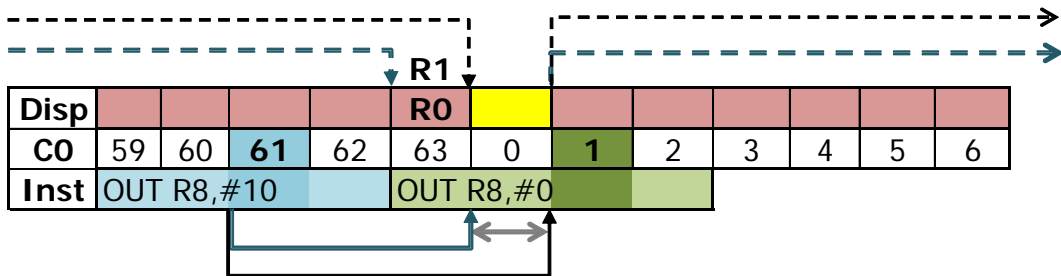
19.2.5.2 SKEW DISP+1 is cancelled on C0=0 : Y GN'EST GNOU ?

The first OUT (R8=#10) prevents the BORDER from being activated on C0=63 (Condition C0=R1 which reports the BORDER for C0=0). However, the 2nd OUT (R8=#00) on C0=0 defines a BORDER OFF on the next character C0=R0. It is considered immediately and cancels the C0=R1 condition programmed on the first OUT.



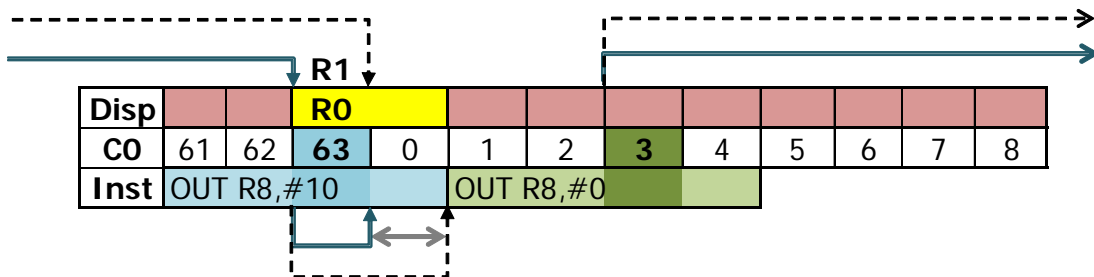
19.2.5.3 SKEW DISP+1 is programmed on C0<63.

The second OUT (R8=#0) occurs too late to prevent the BORDER programmed with the first OUT from being activated on the following character C0=63 (Condition C0=R1 which reports the BORDER for C0=0).



19.2.5.4 SKEW DISP+1 is programmed on C0=63 : COMBO BORDER !

Before being programmed with #10, R8 is equal to 0, and the BORDER was programmed for C0=R1 (i.e. C0=63). Programming R8 with #10 is not fast enough to prevent the BORDER from being activated. However, this programming is considered for the following character, which results in an additional BORDER byte



19.3 INTERLACE FUNCTIONS

19.3.1 GENERAL

The first thing that can be said is that the method of approach on this subject by the various CRTC manufacturers is quite... varied.

This first chapter concerns the principle of operation as it is described (very superficially) in the technical guides of the components. The chapters devoted to this function will be completed in more advanced versions of this document (having not yet finished the analysis of certain results for substantive reasons (ah ah)).

There are 2 programmable interlaced modes on all CRTC's.

The main objective of the interlaced mode is to create a "screen" composed of 2 frames at 50Hz, interlaced, in order to display an image with a doubled vertical resolution. A "complete" image is made up of 2 "frames" of 50 Hz in order to display a complete image at 25 Hz in 625 lines (30 Hz in 525 lines).

To proceed, the CRTC must:

- Be able to create an image composed of 625 distinct lines (on a 50Hz screen)
- Display two frames of 312 lines, plus an additional line.
The length of a frame then being $19968 + 32 = 20000 \mu\text{sec}$.

In order to increase the vertical resolution, the CRTC, during VSYNC, delays the signal by half a line when C4 changes to R7 for the screen displayed with the even lines. When C4 reaches R7, the VSYNC signal from the CRTC is generated taking $C0=R0/2$ as the new reference

If the CRTC communicated directly with the CTM screen, **which is not the case on CPC**, this would have the effect of raising the electron gun half a line higher (-0.5). But an additional line is added at the end of the first screen, which cause to moving the start of the odd screen down one line ($-0.5+1=0.5$) thus allowing the lines to be ordered.

The ability to handle an interlace image depends heavily on the monitor:

- On the one hand on the persistence capacity of phosphors, to limit flickering (which some would call "flashouille" in certain cold and humid French regions).
- On the other hand, on the stability of the high voltage elements of the monitor to limit distortions on the edges of the screen.

On the CPC, the GATE ARRAY merges the HSYNC and VSYNC signals into a composite signal, and the VSYNC is sent along with the HSYNC to the CTM by the GATE ARRAY. However, it is the starting position of the VSYNC during the line that allows to raise the electron gun more or less high (the later the VSYNC starts in the line, the higher the beam goes up).

Since the HSYNC is (in principle) always located in the same place, all the lines displayed on a CTM monitor have a definition of 1 pixel, which contradicts the logic stated above. In the case of a "Standard" CPC screen with $R2=46$ and $R0=63$, the VSYNC generated by the CRTC (on $C0=0$ on the first screen, on $C0=31$ on the second) is retrieved by the GATE ARRAY, which will wait for the 1st μsecond of the 2nd HSYNC to send the signal to the monitor. The electron gun then goes up exactly to the same place as on the previous screen (-0.0).

The additional line generated at the end of the first screen positions the odd screen 1 complete line down (-0.0+1=1). The first line of the even screen then alternates with the additional line, which is quite far from the expected effect.

So in this situation we have:

- 1 even frame with a duration of 19968 μsec, the Vsync not being “shifted”.
- 1 odd frame, which inherits the additional line from the even screen, and lasts 20032 μsec.

Fortunately, this is far from being irremediable (See Chapter 15.3, page 130).

19.3.2 THE TWO INTERLACE MODES

19.3.2.1 INTERLACE SYNC MODE : FUNCTION 00xx0001

This mode is used when you want the CRTIC to display the same information for both the even and the odd screen.

The objective of this mode is to improve the quality of the characters displayed by filling the spaces between the lines in "non-interlace" mode.

In this mode, the CRTIC only increases the resolution by moving the position of the VSYNC signal by 1/2 line, as indicated in the previous paragraph.

The image in this situation uses the same video memory, displaying the same thing twice. In principle, it is not necessary in this mode to reprogram the CRTIC registers. Line 0 of the even lines screen is displayed first, followed by line 0 of the odd lines screen, and so on.

Screen:	Even	Odd	Beautiful drawing							
C9=	0									
C9=		0								
C9=	1									
C9=		1								
C9=	2									
C9=		2								
C9=	3									
C9=		3								
C9=	4									
C9=		4								
C9=	5									
C9=		5								
C9=	6									
C9=		6								
C9=	7									
C9=		7								

19.3.2.2 INTERLACE SYNC & VIDEO MODE : FUNCTION 00xx0011

This **IVM** mode is called "**Video Mode**" because it can be used to display images for which each of the 625 lines is different.

Contrary to the "Interlace Sync Mode", no line from the 2 screens is repeated.

On the first screen, the CRTC displays the lines for which C9 is even.
 On the second screen, the CRTC displays the lines for which C9 is odd.

At the end of the display of the 2 screens (~0.04 second), the lines follow each other in even/odd order.

Given that it is necessary to display twice as many lines, it is therefore necessary to program the registers of the CRTC as if we were building a screen of 624 lines.

This logic has been abused by circuit designers.

The addition of the 625th line is managed automatically by the CRTC, as a reminder.

Note: In the UM6845R documents, the figure (7) used to describe this mode is incorrect (description of the line numbers displayed in the even/odd screens).
 This error does not exist in the UM6845 documents from UMC (figure 13), which is a "confirmed" copy of the HD6845S from HITACHI (and detected as a CRTC 0).

Screen:	Even	Odd	ArtWork from MOMA							
C9=	0									
C9=		1								
C9=	2									
C9=		3								
C9=	4									
C9=		5								
C9=	6									
C9=		7								
C9=	8									
C9=		9								
C9=	10									
C9=		11								
C9=	12									
C9=		13								
C9=	14									
C9=		15								

Due to the repositioning of the sending of the VSYNC by the GATE ARRAY, the even screen is displayed a full line earlier than the odd screen.

In this context, line 0 alternates with a line of BORDER, while line 1 alternates with line 2, line 3 with line 4, and so on...

The image described above thus appears as on the diagram below, the "common" pixels then appearing in their original colours, rather than alternating with the white ink.

C9	Beautiful Drawing Even Screen							
0								
2								
4								
6								
8								
10								
12								
14								

C9	Beautiful Drawing Odd Sceen							
	BORDER or PREVIOUS LINE							
1								
3								
5								
7								
9								
11								
13								
15								

19.3.3 LIMITATIONS

There are specification differences on the registers to be updated (and their value) in Interlace mode between different circuits. These differences are mainly related to the counting mode of C9 and C4 initially defined by the designers of the circuits.

Of course, these restrictions are made not to be respected, but they nevertheless give interesting clues to the inner workings of the counters.

This is particularly the case for the R9 register on CRTCs 0, 3 and 4, which require that R9 be programmed with the number of lines of a vertical character, minus 2 for IVM mode. This should facilitate the end comparison of even lines, because it suffices to ignore bit 0 to perform the end of character comparison and to manage this bit 0 as that of frame parity.

The display of one line out of two causes the faster increment of C4 (on CRTCs 0, 1, 3, 4) and therefore of the VSYNC which occurs when C4=R7. The construction of a screen in the IVM mode therefore requires adapting R4 and R7 to the total size of the desired screen (except for CRTC 2, which adopts another methodology).

When a large screen is defined, it is possible to use "Overscan Bits"™ to avoid having to reprogram R12/R13 between even and odd screens, but I digress.

19.3.4 UNLOVED FEATURE

INTERLACE mode is an unpopular feature with CPC developers.

Note: I should have released demo 4 :-)

However, **this function is managed in real time** and its interest is not only related to its ability to "properly" process an Interlace image but also by producing, via the GATE ARRAY, a useful signal for the monitor.

As soon as the function is activated on a given C9 line, it can affect **the C9 and/or C4 count for the following lines.**

According to the value of C9 and its parity when R8 is modified, then the following line is immediately calculated according to a recipe specific for each CRTC.

In other words, from the perspective of creating a "complete" Interlace screen, **R8 should in principle only be activated when a screen starts** (when C4=C9=0).

From the perspective of using only certain functions of the IVM interlace, it is possible to activate and deactivate this mode before certain functions take place.

Thus, the number of lines of a screen depends on when the Interlace mode was activated, and then contains even and odd lines until the moment when the IVM mode is deactivated, in order to return to a "classic" count.

Activating Interlace mode, in addition to modifying the C9 and C4 count, activates two other distinct managements:

- The **management of one additional line at the end of the first screen**, before $C9=C4=C0=0$. The additional line is added considering that $C5=-1$.
- **Management of activation of the VSYNC signal on $C0=R0/2$ (therefore on $C0=31$ in the case of a screen or $R0=63$)** when $C4=R7$.

19.4 VERTICAL INTERLACE PROGRAMMING

19.4.1 CRTC 0

In **INTERLACE SYNC**, R4, R6 and R7 must be programmed as per a 50Hz screen. R9 must be programmed with the value N-1 if N represents the number of line(s) of a vertical character.

Note that C4 must reach R6 for the additional line to be added between 2 frames. If $R6>R4$, this eliminates the stroboscopic effect of the "CPC" interlace.

In **INTERLACE VIDEOMODE**, R4, R6 and R7 must be programmed as per a 25 Hz screen (which consists of doubling their values compared to that of a non-interlace screen). R9 must be programmed with the value N-2 if N represents the number of line(s) of a vertical character.

For example, if a vertical character is 8 lines long, R9 must contain 6.

CRTC 0 shares this feature with CRTC's 3 and 4.

When an additional interlace line is added, it should be considered as if a line were added to R5. C4 is incremented once and is equal to $C4=R4+1$.

If R9 is programmed with 0, this means that there are at least 2 lines displayed (1 per 50Hz screen).

19.4.2 CRTC 1

If N represents the number of line(s) of a vertical character, then R9 must be programmed with the value N-1 in the 2 interlace modes.

In **INTERLACE SYNC**, R4 and R7 must be programmed as per a 50Hz screen.

In **INTERLACE VIDEOMODE**, R4 and R7 must be programmed with the number of characters of the "total" screen at 25 Hz. This consists of doubling their values compared to a non-interlace screen.

The addition of the additional line does not depend on the equivalence $C4=R6$, unlike CRTC 0 and 2. When the additional line is added, it must be considered that it is as if 1 line is added to R5. C4 is incremented each time $C9=R9$. If $R9+1$ is a multiple of R5, then in interlace mode, C4 is incremented once more on all even screens.

19.4.3 CRTIC 2

If N represents the number of line(s) of a vertical character, then R9 must be programmed with the value N-1 in the 2 interlace modes.

The number of line(s) of a vertical character must however be even (R9 must be programmed with an odd value).

In **INTERLACE SYNC**, R4, R6 and R7 must be programmed as per a 50Hz screen.

In **INTERLACE VIDEOMODE**, R4, R6 and R7 must be programmed as per a 50Hz screen.

Note that C4 must reach R6 for the additional line to be added between 2 frames. If $R6 > R4$, this eliminates the stroboscopic effect of the "CPC" interlace. When the additional line is added, it should be considered as if 1 line is added to R5. C4 is incremented each time $C9 = R9$. If $R9 + 1$ is a multiple of R5, then in interlace mode, C4 is incremented once more on all even screens.

If R7 is programmed with this value of C4, there is no more VSYNC one frame out of 2.

There are therefore situations where C4 is not incremented when $C9 = R9$ but the video pointer is still updated. Thus, R6 concerns 2 characters and not just one, and therefore this is the reason it is "indicated" in the technical documentation that R6 must be even.

19.4.4 CRTIC 3 & 4

In **INTERLACE SYNC**, R4, R6 and R7 must be programmed as per a 50Hz screen. R9 must be programmed with the value N-1 if N represents the number of line(s) of a vertical character.

In **INTERLACE VIDEOMODE**, R4, R6 and R7 must be programmed as per a screen at 25 Hz (which amounts to doubling their value compared to a non-interlace screen). R9 must be programmed with the value N-2 if N represents the number of line(s) of a vertical character.

For example, if a vertical character is 8 lines long, R9 must contain 6.

The addition of the additional line does not depend on the equivalence $C4 = R6$, unlike CRTIC 0 and 2. When the additional line is added, C4 is not incremented. The last value of C4 therefore carries all the additional lines programmed in R9, plus those of R5 and that of the additional line interlace generated during the even screens

19.5 PARITY

19.5.1 GENERAL

When it comes to interlace mode, the screen parity plays an important role because it participates in:

- The addition of the extra line when the construction of the even screen is completed.
- The generation of a Mid-VSYNC when $C4 = R7$ on the even screen.
- Calculation of even and odd C9s.

The common point between all CRTIC's is to have an internal state that switches from even to odd and vice versa according to different conditions.

19.5.2 CRTC 0

The parity state switches between each screen **when $C4=C9=C0=0$ if $C4$ has reached $R6$ during the screen** or at **each new $C4$ when $R9$ is ODD** (odd number of lines for a character in IVM mode).

If $C4$ cannot reach $R6$ (because $R6>R4$) then the parity remains fixed.

The CRTC sets a state when $C4$ reaches $R6$, which is used when $C4=C9=C0=0$ to invert parity. The permutation management of this parity is independent of $R8$.

In **IVM** mode, $R9$ is programmed with an **even** number to define an **even** number of lines in a character (For example $R9=6$ to obtain 2×4 line/char=8 lines). This is related to the method used to test the end of a character composed only of even lines or odd lines depending on the current parity. In this case, the parity is identical regardless of the value of $C4$.

When $R9$ is **odd** in IVM (unlike CRTC 1), this implies a difference between the number of even and odd lines for a character between 2 frames (the total number of lines of a vertical character is odd). In this circumstance, the designers of the circuit balanced the number of lines between 2 frames in order to avoid that there is a screen with $R4+1$ lines more on an even frame than on an odd frame. The adopted solution consists in alternating characters composed of even lines with characters composed of odd lines on the same frame **each time $C4$ evolves**. Thus, when **$R9$ is odd, the parity of the lines depends on that of $C4$ and on the current parity at the start of the frame** (in this sense, if $R4$ is odd, we have an even number of vertical characters, and this implies that the parity does not change at the start of each frame).

It is however possible to wait for precise parity because it is possible to determine, given that there is a counting bug when the IVM mode is activated on $C9=R9$ with an odd parity, or when the IVM mode is deactivated on $C9.VMA=R9+1$ (See next Chapter). Once parity is identified, it suffices to let $C4$ reach $R6$ once for the parity to reverse. The methods are multiple.

The state that allows the CRTC to know if it must generate an additional line is defined when $C4$ reaches $R6$ according to the current parity. If the parity is even, the additional row status becomes true, otherwise it becomes false. The additional line will be added at the end of the screen if one of the two interlace modes is activated ($R8=3$ or 1).

This implies that if this additional row state is true (because we were on an even screen when $C4$ reached $R6$) and on the next (odd) screen $C4$ can no longer reach $R6$, then an additional row will be generated for each screen while $R6>R4$ (and $R8=3$ or 1).

The Mid-VSYNC is generated when $C4=R7$ if the current parity is even.

19.5.3 CRTIC 1

The parity state switches between each frame, as soon as **C4=C9=C0=0**, or at **each new C4 when R9 is EVEN** (odd number of lines for one character).

When R9 is **even**, the number of lines of a vertical character is **odd**. In this circumstance, the designers of the circuit balanced the number of lines between 2 frames in order to avoid that there is a screen with R4+1 lines more on an even frame than on an odd frame.

The adopted solution consists in alternating characters composed of even lines with characters composed of odd lines in the same screen. Thus, when **R9 is even, the parity of the lines depends on that of C4 and on the current parity at the start of the frame** (in this sense, if R4 is odd, we have an even number of vertical characters, and this implies that the parity does not change at the start of each frame).

When R8 is modified (R8 changes from 0 to 3 or vice versa), bit 0 of C9 is updated according to the value of bit 0 of R9=0. This modification of C9 occurs at the **start of the 3rd μsecond of the instruction OUT (C),C (on R8): C9.0=C9.0 xor (C4.0 xor (not R9.0))**

The value of C9 only becomes final **from the 4th μsecond of the OUT(C),C instruction** when R8 goes to 3. The parity switches according to specific conditions.

On the **3rd μsecond**: **Si Parity=0 and C9.0=1 Then InvPar=1 Else InvPar=0**
C9.0=C9.0 xor (C4.0 xor (not R9.0))

On the **4th μsecond**: **Parity=C9.0 xor InvPar**
C9.0=Parity

Thus, if R9 is even, C4 and C9 are odd, C9 will become even on the 3rd μsecond and become odd again on the 4th μsecond.

Example 1 : C9=5, C4=3 and R9=7 (odd). Mode IVM on.

	C0	0	1	2	3	4	5	6	7	8	9
R9=7	C9	5	5	5	5	5	5	4	4	4	4
								OUT R8,3			on

Example 2 : C9=5, C4=3 and R9=7 (odd). Mode IVM off.

	C0	0	1	2	3	4	5	6	7	8	9
R9=7	C9	5	5	5	5	5	5	5	5	5	5
								OUT R8,0			off

Example 3 : C9=3, C4=3 and R9=6 (even). Mode IVM on, then off.

	C0	0	1	2	3	4	5	6	7	8	9	10	11
R9=6	C9	3	3	3	3	3	2	3	3	3	2	2	2
								OUT R8,3			on	OUT R8,0	off

Example 4 : C9=2, C4=3 and R9=6. Mode IVM on, then off.

	C0	0	1	2	3	4	5	6	7	8	9	10	11
R9=6	C9	2	2	2	2	2	3	3	3	3	2	2	2
					OUT R8,3		on	OUT R8,0		off			

If IVM mode is enabled and disabled on the same line when C9=R9, then the parity management state remains "on" in the C9=R9 test for the next character. In other words, this alters, 1 frame out of 2, the possibility for the CRTIC to consider the assignment of VMA' with VMA when C0=R1 and C9=R9.

Given that the parity of a screen used in IVM is fixed each time R8 goes to 3, it is necessary to position it only once if the objective is to use the interlace mode in a "conventional" way, in order to parity swap between each screen.

19.5.4 CRTIC 2

As on CRTIC 0, the parity state switches between each screen when **C4=C9=C0=0 if C4 has reached R6 during the screen**. If C4 cannot reach R6 (because R6>R4) the parity remains fixed. The CRTIC sets a state when C4 reaches R6, which is used when C4=C9=C0=0 to invert parity. The permutation management of this parity is independent of R8.

Unlike all other CRTIC's, the management of C9 is carried out in a simple manner. Parity is respected regardless of the values of R9 and C4.

Parity management for the "calculation" of C9 is considered immediately from the 3rd NOP of OUT(C) on R8:

EVEN PARITY FRAME

C0	0	1	2	3	4	5	6	7	8	9	10	11
C9	3	3	3	3	3	3	3	3	3	3	3	3
C9.Vma	3	3	3	3	3	6	6	6	6	3	3	3
					OUT R8,3		on	OUT R8,0		off		

ODD PARITY FRAME

C0	0	1	2	3	4	5	6	7	8	9	10	11
C9	3	3	3	3	3	3	3	3	3	3	3	3
C9.Vma	3	3	3	3	3	7	7	7	7	3	3	3
					OUT R8,3		on	OUT R8,0		off		

CRTIC 2 may not be able to do SPLITBORDER, but it can do SPLITC9!

The next version of the compendium will address these concepts more specifically for CRTIC 2.

19.5.5 CRTC 3 & 4

The parity state switches between each frame **when C4=C9=C0=0** (as on CRTC 1), or at **each new C4 when R9 is ODD** (as on CRTC 0) (odd number of lines for one character in IVM mode).

In IVM mode, R9 is programmed with an **even** number to define an **even** number of lines in a character (For example R9=6 to obtain 2 x 4 line/char=8 lines). This is related to the method used to test the end of a character consisting of only lines or odd lines according to the current parity. In this case, the parity is identical regardless of the value of C4.

When R9 is **odd** in IVM (as on CRTC 0), this implies a difference between the number of even and odd lines for a character between 2 frames (the total number of lines of a vertical character is odd). In this circumstance, the designers of the circuit balanced the number of lines between 2 frames in order to avoid that there is a screen with R4+1 lines more on an even screen than on an odd screen.

The adopted solution consists in alternating **characters composed of even lines with characters composed of odd lines on the same frame each time C4 evolves**. Thus, when R9 is odd, the parity of the lines depends on that of C4 and on the current parity at the start of the frame (in this sense, if R4 is odd, we have an even number of vertical characters, and this implies that the parity does not change at the start of each screen).

19.6 COUNTING IN INTERLACE VIDEOMODE

19.6.1 CRTIC 0

When **IVM** mode is activated, counter C9 continues to increment normally.

However, when C9 is used in building up the VMA address, C9 is considered shifted left by 1 bit, and bit 0 represents parity. Each increment therefore "corresponds" to an addition of 2 to the counter C9-VMA considering the parity.

The increment management of C9 continues to be processed on the normal value of C9.

From the line C9 which follows that where R8 goes to 3, the value of C9 is multiplied by 2 to be tested with R9 in order to allow C9 to return to 0. The capacity of R9 being 5 bits, the more significant bit is "lost" in the multiplication operation.

We can formulate it like this on the lines located after the one where R8 has gone to 3:

```
If ((C9.Current x 2)+Parity) == (R9+Parity)  
Then  
    Parity = Parity xor (R9 and & 1) (Screen Parity reverted if R9 parity is even)  
    C9.Next=0 ; Management of C4 (C4++ or C4=0)  
Else  
    C9.Next=C9.Current+1  
End If  
If R8=3  
Then  
    C9.VMA=(C9.Next x 2)+Parity  
End If
```

When R8 changes to 3, a status indicates that the calculation of the value compared to R9+Parity will be performed on the next C0=0, after the C9/R9 test of the line. This is most certainly done in this way to prevent the C9 used for the display from switching mid-line. The test value for R9 is therefore the old C9, but the parity is however considered immediately for R9.

Thus, on the line where R8 goes to 3, it is C9 (and not C9.VMA) which is compared to R9+Parity. **If C9=R9 and the parity is odd, then the test C9=R9+1 is false: C9 is not reset to 0 and overflows.** In other words, C9=R9+1.

The value of C9 when R8 goes to 3 can lead to an overflow of C9.

For example, if R9=6 and C9=4 when R8 goes to 3, C9 is different from R9+parity (6 or 7) and the following C9 will therefore be C9+1=5. The C9.VMA displayed (and tested until the end of the line) will be (C9x2)+Parity, i.e. 10 or 11 depending on the current parity. C9 will then continue to increment until C9x2+parity equals R9+parity.

When R8 returns to 0, the same mechanics apply. The state set with R8 is considered when C0 returns to 0. The test takes place with C9.VMA (which includes parity) and R9: Parity is no longer considered for R9. The limit test is therefore carried out with C9x2+Parity (C9.VMA) and R9 (without parity).

Note: The C9/R9 or C9.VMA/R9+Parity test also takes place when C0=R1 (which determines the activation of the BORDER) and the assignment of VMA' with VMA when C9=R9 (or C9.VMA=R9+Parity). Considering parity with R9 as soon as R8=3 (and not taking it into account as soon as R8=0) in the test with C9/C9.VMA can therefore also affect the update of VMA'.

If C9 was 3 and R9=6 on an odd screen, then C9.VMA=7 at the beginning of the line. When R8 goes to 0, C9.VMA is compared to R9 (the consideration of parity is cancelled). C9.VMA=7 <> R9=6, which leads C9 to be incremented (and therefore go to 4). If we wanted C9 to return back to 0, we would for example have to program R9 with C9.VMA before the end of the line (i.e. 7) so that the comparison between C9.VMA and R9 without parity allows C9 to return back to 0.

The diagrams on the following pages describe different counting situations, when switching to IVM mode or when exiting IVM mode. They indicate the value of C9 considered and that available for the constitution of the video pointer.

The IVM period for the following tests covers only a few lines of the screen.

The values of the registers for the indicated results are:

R9=6 (even) and R8=0 before going to 3 (or returning to 0).

Switching to IVM mode on CRTC 0 :

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
1	0	0	
1	1	2	
1	2	4	
1	3	6	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	R8=3
0	2	4	
0	3	6	
1	0	0	
1	1	2	
1	2	4	
1	3	6	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	R8=3
0	3	6	
1	0	0	
1	1	2	
1	2	4	
1	3	6	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	R8=3
0	4	8	
0	5	10	
0	6	12	
0	7	14	
0	8	16	
0	9	18	
0	10	20	
0	11	22	
0	12	24	
0	13	26	
0	14	28	
0	15	30	
0	16	0	
0	17	2	
0	18	4	
0	19	6	
1	0	0	
1	1	2	
1	2	4	
1	3	6	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	R8=3
0	2	5	
0	3	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	R8=3
0	3	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	R8=3
0	4	9	
0	5	11	
0	6	13	
0	7	15	
0	8	17	
0	9	19	
0	10	21	
0	11	23	
0	12	25	
0	13	27	
0	14	29	
0	15	31	
0	16	1	
0	17	3	
0	18	5	
0	19	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	R8=3
0	5	10	
0	6	12	
0	7	14	
0	8	16	
0	9	18	
0	10	20	
0	11	22	
0	12	24	
0	13	26	
0	14	28	
0	15	30	
0	16	0	
0	17	2	
0	18	4	
0	19	6	
1	0	0	
1	2	2	
1	4	4	
1	6	6	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	R8=3
0	5	11	
0	6	13	
0	7	15	
0	8	17	
0	9	19	
0	10	21	
0	11	23	
0	12	25	
0	13	27	
0	14	29	
0	15	31	
0	16	1	
0	17	3	
0	18	5	
0	19	7	
1	0	1	
1	2	3	
1	4	5	
1	6	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	R8=3
0	6	12	
0	7	14	
0	8	16	
0	9	18	
0	10	20	
0	11	22	
0	12	24	
0	13	26	
0	14	28	
0	15	30	
0	16	0	
0	17	2	
0	18	4	
0	19	6	
1	0	0	
1	2	2	
1	4	4	
1	6	6	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	R8=3
0	6	13	
0	7	15	
0	8	17	
0	9	19	
0	10	21	
0	11	23	
0	12	25	
0	13	27	
0	14	29	
0	15	31	
0	16	1	
0	17	3	
0	18	5	
0	19	7	
1	0	1	
1	2	3	
1	4	5	
1	6	7	

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	R8=3
1	0	0	
1	2	2	
1	4	4	
1	6	6	
2	0	0	
2	2	2	
2	4	4	
2	6	6	
3	0	0	
3	2	2	
3	4	4	
3	6	6	
4	0	0	
4	2	2	
4	4	4	
4	6	6	
5	0	0	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	R8=3
0	7	15	
0	8	17	
0	9	19	
0	10	21	
0	11	23	
0	12	25	
0	13	27	
0	14	29	
0	15	31	
0	16	1	
0	17	3	
0	18	5	
0	19	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	

Exit of IVM mode on CRTC 0 :

EXIT IVM MODE ON EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
1	0	0	R8=0
1	1	1	
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
1	0	0	
1	1	2	R8=0
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
1	0	0	
1	1	2	
1	2	4	R8=0
1	3	3	
1	4	4	
1	5	5	
1	6	6	
2	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
1	0	0	
1	1	2	
1	2	4	
1	3	6	R8=0
2	0	0	
2	1	1	
2	2	2	
2	3	3	

EXIT IVM MODE ON ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	1	R8=3
0	1	3	
0	2	5	
0	3	7	
1	0	1	R8=0
1	1	1	
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	1	R8=3
0	1	3	
0	2	5	
0	3	7	
1	0	1	
1	1	3	R8=0
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	1	R8=3
0	1	3	
0	2	5	
0	3	7	
1	0	1	
1	1	3	
1	2	5	R8=0
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	1	R8=3
0	1	3	
0	2	5	
0	3	7	
1	0	1	
1	1	3	
1	2	5	
1	3	7	R8=0
1	4	4	
1	5	5	
1	6	6	
1	7	7	

19.6.2 CRTC 1

The calculation method of C9 is based on two principles. On the one hand an equivalence in number of lines between the even and odd screens, and on the other hand a conservation of the parity of lines.

As a reminder, the parity is fixed when R8=3 according to the parity of R9 when C9 is even. Moreover, if R9 is even (number of lines of an odd character), then the parity is positioned according to the parity of C4.

Below, I will note **p** the screen parity (0=even / 1 odd).

The limit test of C9 is carried out by eliminating bit 0 of C9 and R9 as soon as R8=3:

If (C9.Current & %1111p) == (R9 & %1111p)

Then

p = p xor ((R9 and & 1) xor 1) (screen parity reversed if R9 is even)
C9.Next=p (and C4=C4+1 (or 0 if C4=R4)).

Else

C9.Next=C9.Current.bit 0=p (a) (immediate consideration of parity)
C9.Next=C9.Next+ 2 (b) (add 2 to counter with parity)

End If

Note 1 : The update of R8=3 has an immediate action on C9:

- A first part of the calculation is carried out immediately for the calculation of C9:
C9.Next= (C9.Current and %1111p) as soon as R8=3 (4th nop of OUT)
- The second part of the calculation is performed when C0 goes back to 0:
C9.Next=C9.Next + (1/2) according to the value of R8 (0/3) when C0=0.

Note 2 : If R8 goes to 3, then to 0 on the same line when C9=R9:

- C9 returns to 0 but the limit test of C9 continues to integrate parity until the limit test is satisfied:
C9 limit test: **If C9.Current==(R9 & %1111p)**

As soon as R8 returns to 0, the counting logic resumes normally.

If C9.Current==R9

Then

C9.Next=0 (and C4=C4+ 1 (or 0 if C4=R4))

Else

C9.Next=C9.Current+ 1

End If

The diagrams on the following pages describe different counting situations, when switching to IVM mode or when exiting IVM mode. The IVM period for the following tests covers only a few lines of the screen.

Value of the registers for the indicated results:

R9=7 (odd) and R8=0 before going to 3 (or going back to 0) on the left side.

R9=6 (even) and R8=0 before going to 3 (or going back to 0) on the right side.

Switching on IVM mode on CRTC 1 :

ENTER IVM ON ODD R9 (7)

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	
1	4	
1	6	
2	0	

ENTER IVM ON EVEN R9 (6)

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	1	
1	3	
1	5	
0	0	
0	2	

C4	C9	R8 UPDATE
0	0	
0	1	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	
1	4	
1	6	

C4	C9	R8 UPDATE
0	0	
0	1	R8=3
0	2	
0	4	
0	6	
1	1	
1	3	
1	5	
0	0	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	R8=3
0	4	
0	6	
1	0	
1	2	
1	4	
1	6	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	R8=3
0	4	
0	6	
1	1	
1	3	
1	5	
1	7	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	R8=3
0	4	
0	6	
1	0	
1	2	
1	4	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	R8=3
0	4	
0	6	
1	1	
1	3	
1	5	

ENTER IVM ON ODD R9 (7)

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	R8=3
0	6	
1	0	
1	2	
1	4	

ENTER IVM ON EVEN R9 (6)

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	R8=3
0	6	
1	1	
1	3	
1	5	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	R8=3
0	6	
1	0	
1	2	
1	4	
1	6	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	R8=3
0	6	
1	1	
1	3	
1	5	
1	7	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	
0	6	R8=3
1	0	
1	2	
1	4	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	
0	6	R8=3
1	1	
1	3	
1	5	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	
0	6	
0	7	R8=3
1	0	
1	2	
1	4	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	
0	5	
0	6	
0	7	R8=3
1	1	
1	3	
1	5	

Exit of IVM Mode on CRTC 1 :

EXIT IVM MODE, EVEN C9

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	R8=0
1	1	
1	2	
1	3	
1	4	
1	5	
1	6	
1	7	

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	R8=0
1	3	
1	4	
1	5	
1	6	
1	7	
2	0	

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	
1	4	R8=0
1	5	
1	6	
1	7	
2	0	
2	1	

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	
1	4	
1	6	R8=0
1	7	
2	0	
2	1	
2	2	

EXIT IVM MODE, ODD C9

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	R8=0
1	2	
1	3	
1	4	
1	5	
1	6	
1	7	
2	0	

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	
1	3	R8=0
1	4	
1	5	
1	6	
1	7	
2	0	
2	1	

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	
1	3	
1	5	R8=0
1	6	
1	7	
2	0	
2	1	
2	2	

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	
1	3	
1	5	
1	7	R8=0
2	0	
2	1	
2	2	
2	3	

19.6.3 CRTC 2

It is not necessary to reprogram R4 so that the screen consists of 312 lines (when R4=38 and R9=7). This is also the case when the IVM mode is programmed on a vertical fraction of the screen. C4 is not skewed when R8 is updated, even temporarily.

R7 also does not need to be reprogrammed for the screen to sync.

We can formulate it like this on the lines located after the one where R8 has gone to 3:

```
If (C9.Current == R9)  
Then  
    C9.Next=0 ; Management of C4 (C4++ or C4=0)  
Else  
    C9.Next=C9.Current+1  
End if  
If R8=3  
Then  
    C9.VMA=(C9.Next x 2)+Parity  
End if
```

The update of VMA' with VMA normally takes place when C0=R1 and C9=R9.
But it then occurs on C9=R9/2 and R9

The limit value of C9 is processed by excluding bit 0 of R9 for the test, and the parity of the frame is then added to obtain the final value of C9.

If R8 goes from 0 to 3 when C9 is 5, then C9 goes to 2 on an even frame (3 odd frame).
If R8 goes from 3 to 0 when C9 is 5, then C9 goes to 2 or 6 depending on its position.

In principle, this translation is immediately considered during the creation of the displayed address, including during the line, from position C0 or R8 is modified.

The BORDER is activated when C4=R6. The characters displayed are no longer "associated" with C4 and a value of the counter can then correspond to several characters. A character being considered here when C9=R9 and C0=R1.

The diagrams on the following pages describe different counting situations, when switching to IVM mode or when exiting IVM mode.

Note: The test IVM period covers only a few lines of the screen, after VSYNC, before VSYNC and before C4 reaches R6. R8 is 0 during VSYNC.

R9=7 and R8=0 before going to 3 (or going back to 0).

Switching in IVM Mode on CRTC 2 :

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	R8=3
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	R8=3
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	R8=3
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	R8=3
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	R8=3
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	R8=3
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	R8=3
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	R8=3
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	R8=3
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	R8=3
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	R8=3
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	R8=3
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	
0	7	7	R8=3
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	14	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	
0	1	1	
0	2	2	
0	3	3	
0	4	4	
0	5	5	
0	6	6	
0	7	7	R8=3
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	15	

Exit IVM Mode on CRTC 2 :

EXIT IVM MODE

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	R8=0
1	1	1	
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	R8=0
1	1	1	
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	R8=0
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	R8=0
1	2	2	
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	R8=0
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	R8=0
1	3	3	
1	4	4	
1	5	5	
1	6	6	
1	7	7	

EXIT IVM MODE

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	R8=0
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	R8=0
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	R8=0
1	6	6	
1	7	7	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	R8=0
1	4	4	
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	R8=0
1	5	5	
1	6	6	
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	R8=0
1	6	6	
1	7	7	

EXIT IVM MODE

EVEN FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	R8=0
1	7	7	

ODD FRAME

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	R8=0
1	7	7	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	2	
0	2	4	
0	3	6	
0	4	8	
0	5	10	
0	6	12	
0	7	14	
1	0	0	
1	1	2	
1	2	4	
1	3	6	
1	4	8	
1	5	10	
1	6	12	
1	7	7	R8=0
2	0	0	
2	1	1	

C4	C9	C9-VMA	R8 UPDATE
0	0	0	R8=3
0	1	3	
0	2	5	
0	3	7	
0	4	9	
0	5	11	
0	6	13	
0	7	15	
1	0	1	
1	1	3	
1	2	5	
1	3	7	
1	4	9	
1	5	11	
1	6	13	
1	7	7	R8=0
2	0	0	
2	1	1	

19.6.4 CRTC 3, 4

There is no documentation on the implementation of Interlace on these emulated CRTC's, however the logic is quite simple.

It is important to remember that when R9 is updated with a value less than C9, then C9 goes to 0.

As on CRTC's 0 and 1, activating IVM mode modifies the counting of C4, and therefore requires adapting the values of R4, R6 and R7 according to changes in C4.

For the IVM mode to follow the logic of even/odd lines, it is however necessary to program R9 in **the same way as on a CRTC 0.**

R9 must therefore contain the number of lines of a character minus 2. That is 6 if a character is composed of 8 lines. Otherwise, the management of C9 leads to a change of parity when C9 returns to 0.

As soon as R8 equals 3, this CRTC executes the following C9 management twice (only once otherwise):

If C9 > R9

Then

C9=0 ; C4 Management (If C4=R4, C4=0, else C4++)

Else

C9++

End if

Example : Context R9=7 and C9=6 (line N)

Line N+1	1 st iteration: C9 is incremented a first time: C9=7
	2 nd iteration: C9 is incremented a second time: C9=8
Line N+2	1 st iteration: 1st iteration: C9 is greater than 7. It goes to 0. C9=0 and C4=C4+1
	2 nd iteration: C9 is incremented a second time: C9=1

In the context of my tests, I did not notice the activation of a parity from one frame to the next when R8 remained at 3 under the conditions described below.

The diagrams on the following pages describe different counting situations, when switching to IVM mode or when exiting IVM mode.

Note: The test IVM period covers only a few lines of the screen, after VSYNC, before VSYNC and before C4 reaches R6. R8 is 0 during VSYNC.

Values in red have not (yet) been verified.

I indicate them because the probability is quite high (this subject is vast...).

R9=6 or R9=7, and R8=0 before going to 3 (or going back to 0).

Switching to IVM mode on CRTC 3 & 4 :

R9=7

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
0	8	
1	1	
1	3	
1	5	
1	7	
2	0	
2	2	
2	4	
2	6	
2	8	

R9=6

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
1	0	
1	2	
1	4	
1	6	
2	0	
2	2	
2	4	
2	6	
3	0	
3	2	

C4	C9	R8 UPDATE
0	0	
0	1	R8=3
0	3	
0	5	
0	7	
1	0	
1	2	
1	4	
1	6	
1	8	
2	1	
2	3	
2	5	
2	7	

C4	C9	R8 UPDATE
0	0	
0	1	R8=3
0	3	
0	5	
0	7	
1	1	
1	3	
1	5	
1	7	
2	1	
2	3	
2	5	
2	7	
2	1	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	R8=3
0	4	
0	6	
0	8	
1	1	
1	3	
1	5	
1	7	
2	0	
2	2	
2	4	
2	6	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	R8=3
0	4	
0	6	
0	8	
1	0	
1	2	
1	4	
1	6	
2	0	
2	2	
2	4	
2	6	

R9=7

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	R8=3
0	5	
0	7	
1	0	
1	2	
1	4	
1	6	
1	8	
2	1	
2	3	
2	5	

R9=6

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	4	R8=3
0	6	
1	0	
1	2	
1	4	
1	6	
2	0	
2	2	
2	4	
2	6	
3	0	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	R8=3
0	6	
0	8	
1	1	
1	3	
1	5	
1	7	
2	0	
2	2	
2	4	

C4	C9	R8 UPDATE
0	0	
0	1	
0	2	
0	3	
0	4	R8=3
0	6	
1	0	
1	2	
1	4	
1	6	
2	0	
2	2	
2	4	
2	6	

Exit IVM Mode on CRTC 3 & 4 :

EXIT IVM MODE

R9=7

C4	C9	R8 UPDATE
0	0	R8=3
0	2	
0	4	
0	6	
0	8	
1	1	R8=0
1	2	
1	3	
1	4	
1	5	
1	6	
1	7	
2	0	

R9=6

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	R8=0
1	2	
1	3	
1	4	
1	5	
1	6	
1	7	
2	0	
2	1	

C4	C9	R8 UPDATE
0	8	R8=3
1	1	
1	3	
1	5	
1	7	
2	0	R8=0
2	1	
2	2	
2	3	
2	4	
2	5	
2	6	
2	7	

C4	C9	R8 UPDATE
0	7	R8=3
1	1	
1	3	
1	5	
1	7	
2	1	R8=0
2	2	
2	3	
2	4	
2	5	
2	6	
2	7	
3	0	

C4	C9	R8 UPDATE
0	7	R8=3
1	0	
1	2	
1	4	
1	6	
1	8	R8=0
2	0	
2	1	
2	2	
2	3	
2	4	
2	5	
2	6	

R9=7

C4	C9	R8 UPDATE
0	5	R8=3
0	7	
1	0	
1	2	
1	4	
1	6	R8=0
1	7	
2	0	
2	1	
2	2	
2	3	
2	4	
2	5	

R9=6

C4	C9	R8 UPDATE
0	4	R8=3
0	6	
1	0	
1	2	
1	4	
1	6	R8=0
1	7	
2	0	
2	1	
2	2	
2	3	
2	4	
2	5	

C4	C9	R8 UPDATE
0	2	R8=3
0	4	
0	6	
0	8	
1	1	
1	3	R8=0
1	4	
1	5	
1	6	
1	7	
2	0	
2	1	
2	2	

C4	C9	R8 UPDATE
0	1	R8=3
0	3	
0	5	
0	7	
1	1	
1	3	R8=0
1	4	
1	5	
1	6	
1	7	
2	0	
2	1	
2	2	

C4	C9	R8 UPDATE
0	4	R8=3
0	6	
0	8	
1	1	
1	3	
1	5	R8=0
1	6	
1	7	
2	0	
2	1	
2	2	
2	3	
2	4	

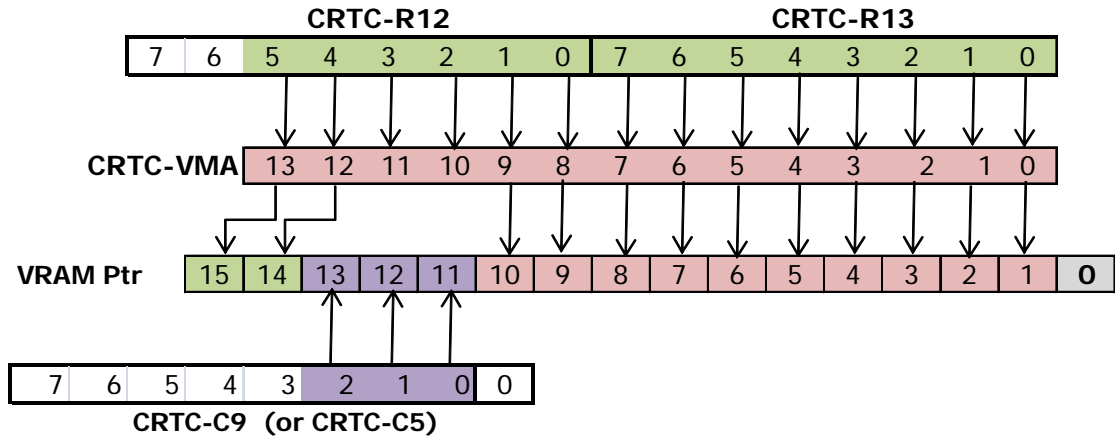
C4	C9	R8 UPDATE
0	3	R8=3
0	5	
0	7	
1	1	
1	3	
1	5	R8=0
1	6	
1	7	
2	0	
2	1	
2	2	
2	3	
2	4	

20 VIDEO POINTER:REGISTERS R12/R13

20.1 GENERAL

These two registers allow for the definition, in conjunction with C9 (or C5), of the base memory address given by the CRTIC to the GATE ARRAY in order for it to display its characters.

20.2 VIDEO POINTER CALCULATION



Bit 0	Always at 0 because the CRTIC works in words
Bits 1 to 10	From bits 0 to 9 of CRTIC-VMA
Bits 11 to 13	From bits 0 to 2 of C9 (or C5 when there is a vertical adjustment with CRTIC 3 and 4)
Bits 14 and 15	From bits 12 and 13 of CRTIC-VMA

When the VMA/VMA' update conditions are met, then VMA or VMA'=R12/R13.
See Chapter 14, page 114.

20.3 UPDATE CONDITIONS

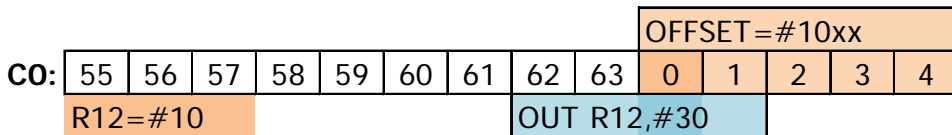
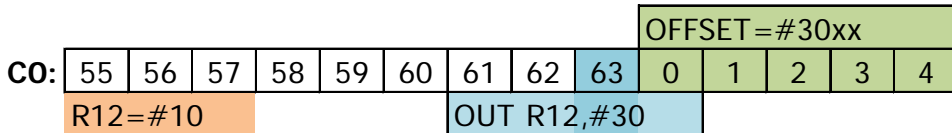
20.3.1 CRTC 0

When the counters C4, C9 and C0 change to 0, the video pointers (VMA' & VMA) are initialized with R12/R13.

Note that if the "screens" are 2 μ sec ($R4=R9=0$ and $R0=1$) then C4 passes through the values 0 and 1 alternately, allowing R12 and/or R13 to be considered every 4 μ s.

(This is the triggering of the "R5" additional line management, which generates a line despite $R5=0$, and therefore increments C4 despite $R4=0$).

The updates of R12 and R13 are considered immediately.



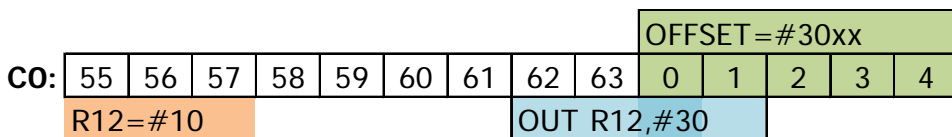
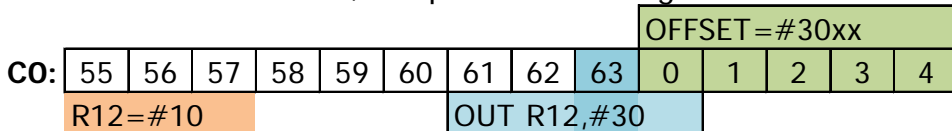
On CRTC 0, **VMA' & VMA are loaded with R12/R13 if C4=0 and C0=0.**

20.3.2 CRTC 1

When C0 and C9 go to 0 and C4=0, the VMA video pointer is initialized with R12/R13.

Note that the update of both R12 and R13 are immediate.

If the conditions are met, it is possible to change the offset on screens of 1 μ s ($R0=0$).



On CRTC 1, **VMA is loaded with R12/R13 while C4=0.**

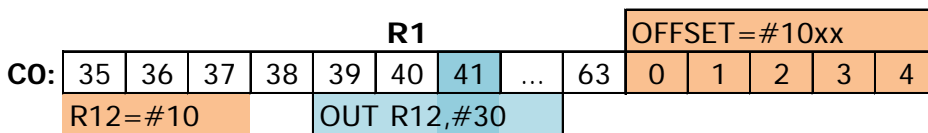
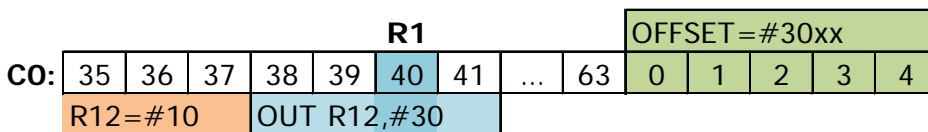
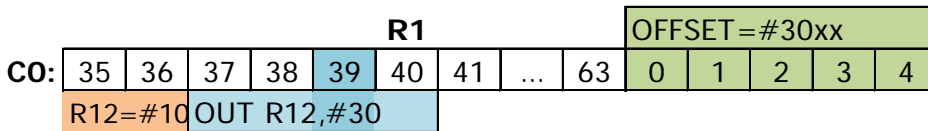
20.3.3 CRTC 2

When counters C4, C9 and C0 change to 0, pointer VMA' is initialized with R12/R13.

Unlike other CRTC's, it is VMA' which is updated with R12/R13.

As a reminder, VMA' is the transient pointer updated when C0 reaches R1, and which updates VMA when C9=R9.

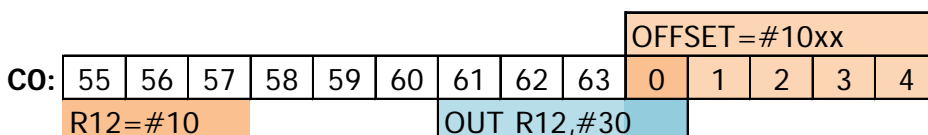
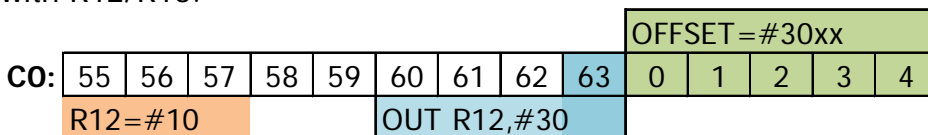
If the update of the R12/R13 registers is immediate, the consideration of the new line can no longer take place when C0 exceeds R1



On CRTC 2, VMA' is loaded with R12/R13 if C4=0 and C0=0.

20.3.4 CRTC 3 & 4

When the counters C4, C9 and C0 change to 0, the video pointers (VMA' & VMA) are initialized with R12/R13.



On CRTC 3 and 4 VMA' & VMA are loaded with R12/R13 if C4=0 and C0=0.

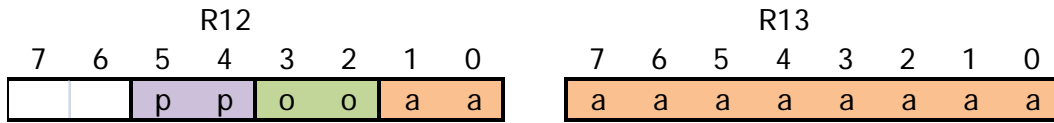
20.4 Deadlines

See the chapter on the R0 register for the precise detail of the update of the video pointer.

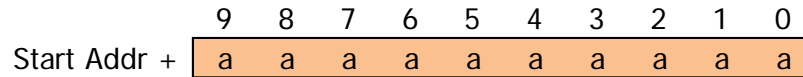
20.5 OVERSCAN-BITS

The construction of the memory address is specific insofar as:

- Bits from C9/C5 are "immovable" in the final pointer.
- The internal address counter counts on 14 bits where bits 10, 11 and 12 are not "used" (at least in appearance).



p	p	Start address	o	o	Managed size
0	0	&0000	0	0	16 k
0	1	&4000	0	1	16 k
1	0	&8000	1	0	16 k
1	1	&C000	1	1	32 k



When R12 and R13 are transferred to VMA/VMA', VMA is used to display the characters.

Although bits 11, 12 and 13 of the final pointer come from C9 (or C5), the VMA counter counts on 14 bits. Also, when the counting reaches the end of 10 address bits, bits 2 and 3 coming from R12 take part in the counting, even if they are not used directly for the video pointer.

If these bits are both at 1, this causes a report on bits 4 and 5 of R12. These 2 bits represent bits 14 and 15 of the video pointer.

The consequence is therefore a change of page when the end of the 10 bits is reached.

It is therefore possible to display an image of more than 16k without resorting to a rupture with this method.

21 READ REGISTERS.

21.1 GENERAL

There are two types of reading possible on the CRTC's.

The first type aims to retrieve the value contained in certain CRTC registers. According to the CRTC's, this reading does not concern the same registers and the same ports.

The purpose of the second type is to retrieve the status of certain internal CRTC operations in order to communicate on the fulfilment of various conditions. Reading statuses does not exist on all CRTC's and does not use the same type of reading.

21.2 READING THE CONTENTS OF THE REGISTERS

In order to be able to read the contents of a register, it must first of all be selected.

As a reminder, an I/O port is selected with the I/O address &BC00.

21.2.1 CRTC 0

Only the 5 least significant bits of the register number are considered. The other 3 most significant bits are ignored. This CRTC is able to read the contents of the following registers on the port located at &BF00:

Register	Definition	Unit	r/w	7	6	5	4	3	2	1	0
R12	Display start address (High)	Pointer	r/w	0	0						
R13	Display start address (Low)	Pointer	r/w								
R14	Cursor address (High)	Pointer	r/w	0	0						
R15	Cursor address (Low)	Pointer	r/w								
R16	Light Pen (High)	Pointer	r	0	0						
R17	Light Pen (Low)	Pointer	r								

Note : The cursor is not managed on the CPC. However, it is perfectly possible to store values in R14 and R15 and then read them back.

An attempt to read another register (0 to 255) returns the value 0.

21.2.2 CRTC 1, 2

Only the 5 least significant bits of the register number are considered. The other 3 most significant bits are ignored. These CRTC's can read the contents of the following registers on the port located at &BF00:

Register	Definition	Unit	r/w	7	6	5	4	3	2	1	0
R14	Cursor address (High)	Pointer	r/w	0	0						
R15	Cursor address (Low)	Pointer	r/w								
R16	Light Pen (High)	Pointer	r	0	0						
R17	Light Pen (Low)	Pointer	r								

Note : The cursor is not managed on the CPC. However, it is perfectly possible to store values in R14 and R15 and then read them back.

For CRTC 2, an attempt to read another register (0 to 255) returns the value 0.

For CRTC 1, an attempt to read another register returns 0, except for register 31 (and all values whose bits 0-4 are 1) which returns a non-zero value (I got 127 or 255). This register was probably defined by UMC but not used on this model.

21.2.3 CRTC 3, 4

For CRTC's 3 and 4, only the 3 least significant bits of the selected register number are considered to read a register according to the following table.

Reading register 4 therefore also means reading register 12 (8+4) or 20 (16+4)

Reading a CRTC register is possible on two I/O addresses indistinctly: &BE00 and &BF00

Note that the "Register Status" port has the same function as the "Register Read" port. These CRTC's nevertheless manage an impressive collection of statuses. The designers used the R10 and R11 registers for this purpose (see next chapter on the statuses).

These CRTC's can read the contents of the following registers:

Nb	Register	Definition	Unit	r/w	7	6	5	4	3	2	1	0
0	R16	Light Pen (High)	Pointer	r	0	0						
1	R17	Light Pen (Low)	Pointer	r								
2	R10	Asic CRTC Status 1	Function	r								
3	R11	Asic CRTC Status 2	Function	r								
4	R12	Display start address (High)	Pointer	r/w								
5	R13	Display start address (Low)	Pointer	r/w								
6	R14	Cursor address (High)	Pointer	r/w	0	0						
7	R15	Cursor address (Low)	Pointer	r/w								

Note : The cursor is not managed on the CPC. However, it is perfectly possible to store values in these registers and then read them back, including both CRTC's 3 and 4.

21.3 READING STATUS

21.3.1 GENERAL

Only CRTC 1 has a status register present on the specific port &BE00.

This port is a mirror of the read port for CRTC's 3 and 4, which handle status differently.

CRTC	7	6	5	4	3	2	1	0
0	x	x	x	x	x	x	x	x
1	x	L	V	x	x	x	x	x
2	x	x	x	x	x	x	x	x
3	d	d	d	d	d	d	d	d
4	d	d	d	d	d	d	d	d

High impedance

High impedance

L	
1	Light pen reading
0	R16 / R17 registers can be read
V	
1	BORDER R6 is true
0	BORDER R6 is false

d : Mirror of BF00 port (read of CRTC reg)

Other CRTC	7	6	5	4	3	2	1	0
UM6845E	U	L	V	x	x	x	x	x
R6545E	U	L	V	x	x	x	x	x

U	
1	Update event
0	Reg R31 has been read / written by the MPU

21.3.2 CRTC 0, 2

These two CRTC's **do not have** a status register.

Therefore, it is not recommended to use the value read on port &BE00 on CRTC's 0 and 2, particularly to test the type of CRTC (risk of Candy Crush).

My CPC CRTC 2 always returns 255 read on this port.

My CPC CRTC 0 randomly returns 255 or 127 on this port.

21.3.3 CRTC 1

The input/output address of the status register on this CRTC is &BE00.

On CRTC 1, bit 5 of the Status register is updated when C0=R0 according to the BORDER R6 conditions (False: C4=C9=C0=0 / True: C4=R6 & C9=C0=0).

The bit is 1 when the BORDER R6 condition is true.

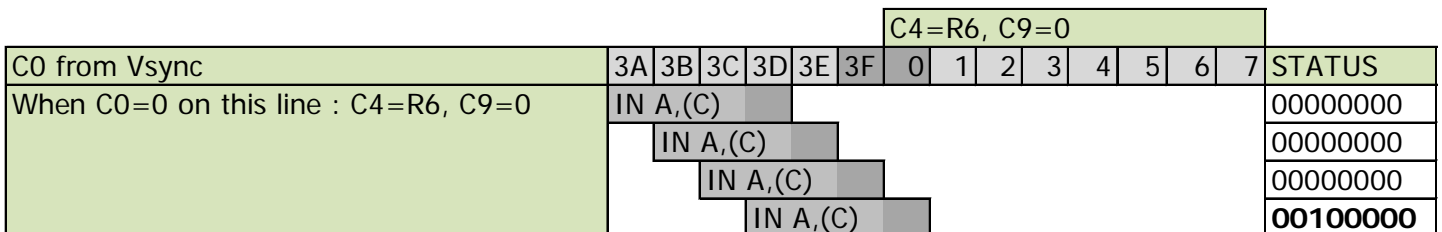
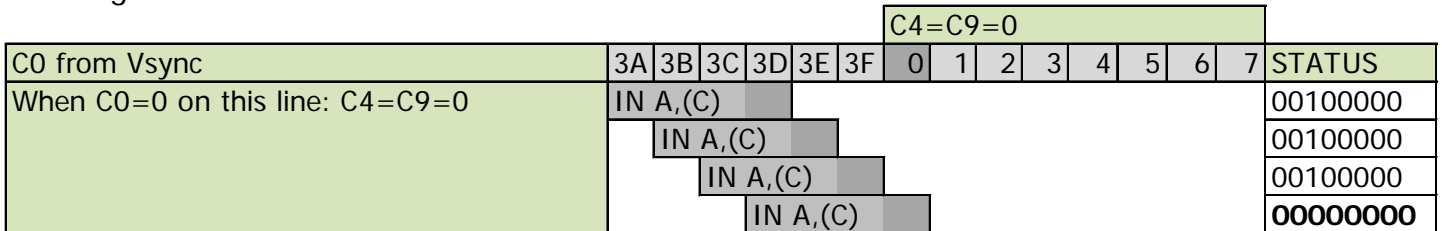
The bit is 0 when the BORDER R6 condition is false.

This does not necessarily mean that BORDER or CHARACTERS are displayed, because this evaluation is done when C0=R0.

But BORDER can already be displayed if the BORDER R1 condition is true.

Note also that if R6 is positioned at 0 (while C4>0) to generate BORDER, this state is not detected. The value 0, like in other CRTC 1 registers, is handled in a special way. In other words, if R6=0 while C4>0 and the status is 0 (Characters displayed), bit 5 of the status register will continue to be 0.

The diagrams below describe the exact transition to 1 or 0 of this status bit.



21.3.4 CRTC 3, 4

The designers of these ASIC's used R10 and R11 as status registers in order to trace a large number of events. It is therefore possible to wait for very precise events and to calculate quite simply the value of all the CRTC registers which are read-only.

The first identification of these statuses was made on CPC PLUS by Kevin THAKER (ArnoldEmu) who refers to them here: <http://cpctech.cpc-live.com/docs/cpcplus.html>
 However, it was a mistake to state that these statuses do not exist on CRTC 4.

Reading these statuses requires great precision because several bits only change state for 1 µsec. In this case, if the status register is read with an **INI** or **IND** instruction, the I/O is read and written in RAM during the 4th µsecond of the instruction (which takes 5). When the register is read with the instruction **IN reg8,(C)**, the I/O is read during the 4th µsecond of the instruction (which takes 4). It is therefore necessary to perfectly calibrate the read instructions so that the 4th µsecond is located at the exact moment when the status is set by the CRTC.

Note : Since bit 3 of the register number is forced to 1, reading registers R2 and R3 is equivalent to reading R10 and R11.

21.3.4.1 Definition of STATUS 1

STATUS 1 (CRTC-R10)								
Bit number	Bit Value	Event						
0	1	C0=R0						
1	0	C0=R0/2						
2	0	C0=R1-1						
3	0	C0=R2						
4	0	C0=R2+R3						
5	0	C0=0..R0 on last Vsync Line						
6	1	Always 1						
7	0	On some specific C0 values for some C4 values :						
		Line from Vsync, to...	C0	C4 start	C9start	C9end	Note	
		8	15	39	31	0	7	R7=30
		15	22	63	32	7	6	
		56	63	55	37	0	7	
		64	71	15	38	0	7	R4=38
		72	78	63	0	0	6	
		112	119	55	5	0	7	
		120	127	15	6	0	7	
		168	175	31	12	0	7	
		216	223	47	18	0	7	
		224	231	7	19	0	7	
		272	279	23	25	0	7	

Bit 1 of this status is set to 0 when C0=R0 >> 1.

The CRTC just considers that bit 0 of the value compared with C0 starts on bit 1 of R0.

21.3.4.2 Definition of STATUS 2

STATUS 2 (CRTC-R11)		
Bit number	Bit Value	Event
0	0	C4=R4 and C9=R9 and C0=R0 : Last char of screen
1	0	C4=R6-1 and C9=R9 and C0=R0 : Last char displayed
2	0	C4=R7-1 and C9=R9 and C0=R0 : Last char before Vsync
3	0	see below
4	1	Always 1
5	0	C9=R9 : Status=0 for C0=0 to R0
6	0	Always 0
7	1	(C9=R9 and C0=63) or (C9=0 and C0=0 to R0-1)

On CRTC 4, the value of bit 3 changes every μ second of the frame on a specific frame in periods of 6 μ seconds: **0, 0, 1, 0, 1, 1**

On CRTC 3, there are 2 different frames.

A first frame of 3 μ seconds which starts from C0vs to the last character of the screen (C4=R4, C9=R9 and C0=R0): **0, 0, 1**

A second frame, identical to that of CRTC 4, which starts from the new screen (C4=0, C9=0, C0=0) up to the first character of the Vsync: **0, 0, 1, 0, 1, 1**

21.4 DUMMY REGISTER

Among some of the myths and legends about CPC CRTC's is the existence of Register 31, called the DUMMY REGISTER.

If register 31 does exist on the CRTC UM6845E from the company UMC, **it does not exist** on the CRTC UM6845R (type 1), nor on the CRTC UM6845 (type 0).

On the CRTC UM6845R, bit 7 of the status register which refers to it is simply unused.
On the CRTC UM6845, the status register itself does not exist (hence finding its bit 7...).

However, it should be noted that reading this register on a CRTC UM6845R (type 1) returns a non-zero value, unlike the other read-only registers.

On the CRTC UM6845E (excluding CPC), register 31 is related to the transparent mode.

The management of this mode also uses bits 6 and 7 of register 8 in addition to bit 7 of the status register. I will not dwell on this subject, which is as interesting as the programming of the EF9345P...

22 FULLSCREEN & CENTERING

22.1 Foreword

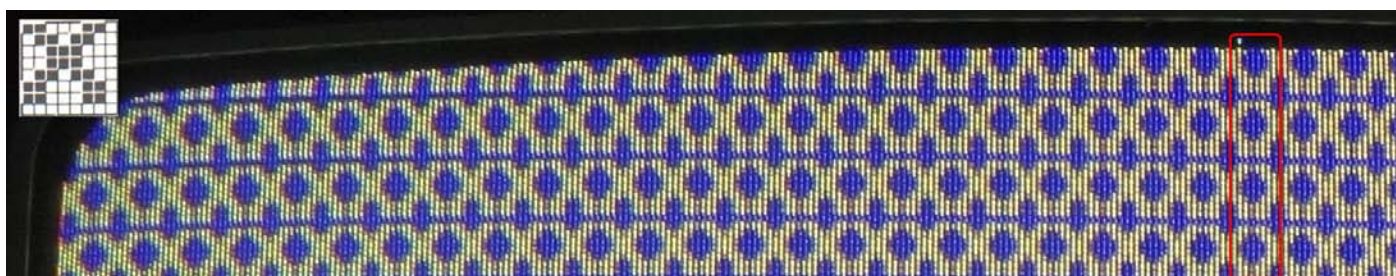
CPC CRT screens are convex with quite a noticeable screen curvature.

Because of this shape and the deflection angle of the electron beam, the pixels at the edges are larger than those at the centre.

In addition, the case that surrounds the cathode ray tube has rounded corners and edges that "roughly" follow the shape of the cathode ray tube, but however masks a few additional pixels in passing. The data given in this chapter corresponds to the general case. Due to the analog nature of the screens, there may be some small variations in size or positioning between 2 screens. Let's not forget that the CPC is over 30 years old.

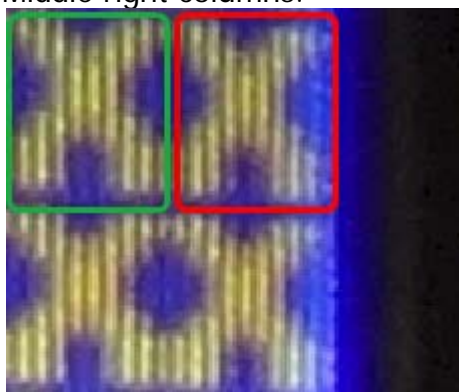
You can see the differences of several horizontal pixels and vertical lines between the centre of the screen and the edges of the latter.

Vertically, a difference of 5 lines can exist between the first line visible in a corner and the first line visible in the middle of the horizontal axis of the screen:

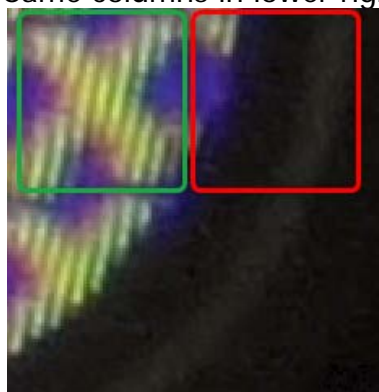


Horizontally, a difference of almost 1 CRT character can be observed between a column located at the top or bottom side corner of the screen and this same column in the middle of the vertical axis of the screen (line 136):

Middle right columns.



Same columns in lower right corner.



It is by counting the number of horizontal characters and vertical lines from the middle of the horizontal and vertical axes of the screen that we can determine the values to be programmed to ensure that all the pixels visible on the screen are "filled". However, keep in mind that many pixels in these rows and columns will not be visible.

22.2 HORIZONTAL FULLSCREEN

On a CTM monitor, one can visualize a horizontal line of **48 CRTC characters**, which represents 96 bytes (192 pixels mode 0, 384 pixels mode 1, 768 pixels mode 2).

The centering of a horizontal line depends on the HSYNC signal (See Chapter 16, page 133).

The first character visible on the left is the 15th character from position $C0=R2$.

To obtain an exact centering on a line of 64 μ sec ($R0=63$), $R2$ must be set to 50 (with $R3 \geq 6$) to display $C0=0$ at the extreme left of the screen.

Depending on the H-HOLD setting of the monitor (accessible via a small flat screwdriver in the small hole at the rear left of the monitor), the BORDER may appear on the right or on the left if the line size is set to 48 characters.

If $R3$ is less than 6, then the screen is shifted to the right (See Chapter 14.4, page 116).

22.3 VERTICAL FULLSCREEN

On a CTM monitor, you can see **272 vertical lines** at 50 Hz (and much more with "homemade" interlace by lowering the frequency, but that's another subject).

The image begins to be visible from the **34th line**, which is the second line of the 5th character of 8 lines from the start of the VSYNC. (See Chapter 15, page 126).

If $R7$ is positioned with 35 while $R4=38$ (and $R5=R8=0$), then 33 "not visible" lines will be generated from the VSYNC, and the line $C4=0/C9=1$ will be partially visible.

23 TIPS AND TRICKS

As soon as it is necessary to modify the registers of several circuits, the 64 μ sec of a line is often an important constraint to respect. Several tricks save valuable μ sec. The main optimizations reside in the economical use of Z80A registers, the method of access to Inputs-Outputs or the management of iterations. These 3 approaches can be combined at will.

23.1 R12/R13 UPDATES

When it is a question of frequently modifying the values of the registers of certain circuits, it is for example not always necessary to modify the 2 registers R12/R13 when certain tricks are time critical, in general for demos.

It is possible to affect only one or the other, or even separately depending on the memory architecture of what must be displayed.

The access mode to the CRTC, which involves the prior selection of a register, is very CPU intensive. (Everything being relative...). An option to minimize the access time to these two registers is to use the **OUT (nn),A** instruction with all the reservations surrounding the use of this malicious instruction on a CPC

Example 1 :

The following code, for example, is used to initialize the pair R13/R12 quickly (considering of course the preloading of the registers). The principle is to allow the selection of a CRTC register without manipulating B several times to switch to the data writing function of the circuit.

Prerequisite : B=&BC, A=12, C=13, H=R12, L=R13

(optionally, SP=&BABA)

```
OUT (C),C ; Select R13  
INC B ; B=Crtc Data Address  
OUT (C),L ; R13=L  
OUT (#FF),A ; Select R12 (12="combo" CRTC Reg Select & Value Reg Select)  
OUT (C),H ; R12=H
```

It is possible to select CRTC registers 8, 4 and 0 with this method. However, the last two values also send the value of register A to port A of the PPI

Example 2 : R0=0

```
LD B,#BD ; B=Crtc Data Address  
XOR A  
OUT (#FF),A ; Select R0  
OUT (C),A ; or OUT(C),0 (see Chapter 23.4)
```

23.2 COMMON USE OF REGISTER(S)

In an effort to save valuable Z80A registers, a few tricks are to put the value of the Input/Output ports or the value of the select registers into registers that also serve as pointers to tables. However, this limits access to tables whose most significant, for example, is a valid value for the circuit.

However, this poses a significant constraint on the organization of memory.

For example, it is possible to place in memory at addresses &BC00, &BD00, &BE00, &7F00 tables containing useful values.

Example 1 :

```
LD B,#BD      ; BC is both CRTC write port
LD A,(BC)     ; and pointer to the value to write (indexed by C here)
OUT (C),A
```

Example 2:

```
LD B,#BE      ; BE is CRTC write port (via OUTI)
LD H,B        ; But also pointer to the value to write (indexed by L)
OUTI          ; HL being also incremented in the operation
```

This sport can also apply to selection registers, such as 12 when it comes to modifying R12 for example.

```
LD B,#BC
LD H,#0C      ; HL is a pointer to a table between #0C00 and #0CFF
OUT (C),H    ; But H also serves as a CRTC register selector
INC B
INC B
OUTI          ; The value present at address #0Cxx is sent to R12
```

23.3 WAITING VSYNC

It is sometimes interesting that B is already preloaded at the end of a "traditional" VSYNC wait. It is possible to use the **IN A,(#FF)** instruction to avoid B being involved, but this involves reloading A with the I/O address of Port B (PPI) at each iteration:

WSYNC	LD A,#F5		LD B,#F5
	IN A,(#FF)	WSYNC	IN A,(C)
	RRA		RRA
	JR NC,WSYNC		JR NC,WSYNC

By loading A using another preloaded 8-bit register, the loop then occupies the same time as a "standard" loop with B because **IN A,(#FF)** executes in 3 μ seconds

23.4 ZERO VALUE

There is an interesting undocumented instruction (**#ED,#71**) that sends the value 0 to the I/O address present in register B: **OUT (C),0**.

In principle, the value sent by this instruction depends on the type of MOS logic of the Z80A. On a NMOS variant, 0 is sent, however on the Z80 CMOS variant, it is the value 255 which is sent.

Example :

```
LD BC,#BC09   ; See Chapter 12.4.1, page 87
OUT (C),C
INC B
OUT (C),C
OUT (C),0
```

23.5 OUTI/OUTD AND STATUS REGISTER

The official documentation is incorrect regarding the N and C bits of the Z80A F register for the OUTI and OUTD instructions. (This is probably also the case for OTIR and OTDR, but of limited interest on the CPC). When the sum of the value sent (in HL) to the circuit and the register L (post processing (incremented/decremented)) is greater than 255, then N=C=1. This potentially allows to test the end of a table without a counter, but it creates a constraint on the address of the table.

23.6 CONDITIONAL ITERATIONS AND BRANCHING

When no further optimization is possible, a widely used method is to eliminate loop branch tests and instructions. However, this can lead to a significant increase in the ram required.

Instead of dealing with conditional branches, another common method is to use a list of execution pointers via the stack. Each RET instruction (3 μ sec) causing the PC register to switch to a new routine (and SP to point to the next address). This method generally requires preparing the table upstream, particularly to manage exit cases if this is not provided for elsewhere. This method nevertheless prohibits the use of interrupts (which of course you have foreseen).

Another method is to use the valuable JP HL, JP IX or JP IY instructions.

The first of these 3 instructions execute in 1 μ sec (the other 2 with 1 μ sec more). L, LX or LY can be used as an index provided, they remain in a 256 byte page.

Note: The ZILOG JP (HL/IX/IY) notation is misleading, because the jump takes place at the address contained in the HL/IX/IY register and not at the address contained at the address pointed to by HL/IX /IY. Recent assemblers accept these new notations.

Finally, and this is very anecdotal, but it is always possible to use CPC interrupts and arrange for R52 to generate an interrupt in order to interrupt a loop, considering that a non-repetitive instruction is not divisible.

23.7 WASTING TIME...

When it is a question of waiting in a precise way, it is possible to use a series of NOP's (1 μ sec) but this can considerably lengthen the code present in ram. If the goal is to minimize the size of a loop in ram, there are a few more or less "register neutral" instructions that take up little space and wait longer than the NOP instruction.

Beware of interrupts and stack contents (or registers) when data neutrality is handled with stack pointer associated instructions.

Instruction (s)	Duration (in μ sec)	Size (in bytes)	Be careful !
NOP	1	1	
CP (HL)	2	1	Update F
JR \$+2	3	2	
INC HL + DEC HL	4	2	
INC (HL) + DEC (HL)	6	2	Update F
PUSH HL + POP HL	7	2	Update stack content
EX (SP),HL + EX (SP),HL	12	2	

24 DURATION OF INSTRUCTIONS ON THE CPC

The Z80A is interrupted by the GATE ARRAY via its READY pin when it reads the 2 bytes of the ram addressed by the CRTIC every μ -second. The Z80A tests the state of its WAIT pin according to the definition of the different cycles of the instruction when it needs to access the ram or perform an input-output.

The WAIT pin (#24) of the Z80A is driven low for 3 out of 4 cycles, causing each memory access to align when the WAIT signal is high again.

The following table describes the Z80A instruction duration in μ seconds.

Instruction	µs	Size		Instruction	µs	Size
ADC A,(HL)	2	1		DI	1	1
ADC A,(IX/IY+d)	5	3		EI	1	1
ADC A, A/B/C/D/E/H/L	1	1		EX (SP),HL	6	1
ADC A,HX/LX/HY/LY	2	2		EX (SP),IX/IY	7	2
ADC A,d	2	2		EX AF,AF'	1	1
ADC HL,BC/DE/HL/SP	4	2		EX DE,HL	1	1
ADD A,(HL)	2	1		EXX	1	1
ADD A,(IX/IY+d)	5	3		HALT	1	1
ADD A, A/B/C/D/E/H/L	1	1		IM m	2	2
ADD A, HX/LX/HY/LY	2	2		IN A/B/C/D/E/H/L,(C)	4	2
ADD A,d	2	2		IN A,(d)	3	2
ADD HL,BC/DE/HL/SP	3	1		IN F	4	2
ADD IX,BC/DE/HL/SP	4	2		INC (HL)	3	1
ADD IY,BC/DE/HL/SP	4	2		INC (IX/IY+d)	6	3
AND A,(HL)	2	1		INC A/B/C/D/E/H/L	1	1
AND A,(IX/IY+d)	5	3		INC HX/LX/HY/LY	2	2
AND A, A/B/C/D/E/H/L	1	1		INC BC/DE/HL/SP	2	1
AND A, HX/LX/HY/LY	2	2		INC IX/IY	3	2
AND A,d	2	2		IND	5	2
BIT x,(HL)	3	2		INDR	6/5	2
BIT x,(IX/IY+d)	6	4		INI	5	2
BIT x, A/B/C/D/E/H/L	2	2		INIR	6/5	2
CALL cond,aa	5/3	3		JP aa	3	3
CALL aa	3	3		JP cond,aa	3	3
CCF	1	1		JP HL	1	1
CP A, (HL)	2	1		JP IX/IY	2	2
CP A, (IX/IY+d)	5	3		JR a	2	2
CP A, A/B/C/D/E/H/L	1	1		JR cond,a	2/3	2
CP A, HX/LX/HY/LY	2	2		LD (BC/DE),A	2	1
CP A,d	2	2		LD (HL),A/B/C/D/E/H/L	2	1
CPD	4	2		LD (HL),d	3	2
CPDR	6/4	2		LD (IX/IY+d), A/B/C/D/E/H/L	5	3
CPIR	6/4	2		LD (IX/IY+d),d'	6	4
CPI	4	2		LD (aa),A	4	3
CPL	1	1		LD (aa),BC/DE/SP/IX/IY	6	4
DAA	1	1		LD (aa),HL	5	3
DEC (HL)	3	1		LD A,(BC/DE)	2	1
DEC (IX/IY+d)	6	3		LD A/B/C/D/E/H/L,(HL)	2	1
DEC A/B/C/D/E/H/L	1	1		LD A/B/C/D/E/H/L,(IX/IY+d)	5	3
DEC HX/LX/HY/LY	2	2		LD A,(aa)	4	3
DEC BC/DE/HL/SP	2	1		LD A/B/C/D/E/H/L, A/B/C/D/E/H/L	1	1
DEC IX/IY	3	2		LD HX/LX,B/C/D/E/HX/LX	3	3
LD HY/LY,B/C/D/E/HY/LY	3	3		RRA	1	1
LD BC/DE/HL/SP,dd	3	3		RRC (HL)	4	2
LD IX/IY,dd	4	4		RRC (IX/IY+d)	7	4
LD BC/DE/HL/SP/IX/IY,(aa)	6	4		RRC(IX/IY+d),A/B/C/D/E/H/L	7	4
LD HL,(aa)	5	3		RRC A/B/C/D/E/H/L	2	2
LD I,A	3	2		RRCA	1	1
LD R,A	3	2		RRD	5	2
LDD	5	2		RST 0/8/10h/18h/28h/30h/38h	4	1
LDDR	6/5	2		SBC A,d	2	2

Instruction	µs	Size	I/O	Instruction	µs	Size
LDI	5	2		SBC A,(HL)	2	1
LDIR	6/5	2		SBC A,(IX/IY+d)	5	3
NEG	2	2		SBC A, A/B/C/D/E/H/L	1	1
NOP	1	1		SBC A, HX/LX/HY/LY	2	2
OR A,(HL)	2	1		SBC HL,BC/DE/HL/SP	4	2
OR A,(IX/IY+d)	5	3		SCF	1	1
OR A, A/B/C/D/E/H/L	1	1		SET x,(HL)	4	2
OR A, HX/LX/HY/LY	2	2		SET x,(IX/IY+d)	7	4
OR A,d	2	2		SET x,(IX/IY+d),A/B/C/D/E/H/L	7	4
OTDR	6/5	2	5*	SET x,A/B/C/D/E/H/L	2	2
OTIR	6/5	2	5*	SLA (HL)	4	2
OUT (C),A/B/C/D/E/H/L	4	2	3	SLA (IX/IY+d)	7	4
OUT (C),0	4	2	3	SLA (IX/IY+d),A/B/C/D/E/H/L	7	4
OUT (d),A	3	2	3	SLA A/B/C/D/E/H/L	2	2
OUTD	5	2	5*	SLL (HL)	4	2
OUTI	5	2	5*	SLL (IX/IY+d)	7	4
POP AF/BC/DE/HL	3	1		SLL (IX/IY+d),A/B/C/D/E/H/L	7	4
POP IX/IY	4	2		SLL A/B/C/D/E/H/L	2	2
PUSH AF/BC/DE/HL	4	1		SRA (HL)	4	2
PUSH IX/IY	5	2		SRA (IX/IY+d)	7	4
RES x,(HL)	4	2		SRA A/B/C/D/E/H/L	2	2
RES x,(IX/IY+d)	7	4		SRL (HL)	4	2
RES x,(IX/IY+d),A/B/C/D/E/H/L	7	4		SRL (IX/IY+d)	7	4
RES x, A/B/C/D/E/H/L	2	2		SRL (IX/IY+d),A/B/C/D/E/H/L	7	4
RET	3	1		SRL A/B/C/D/E/H/L	2	2
RET cond	2/4	1		SUB A,(HL)	2	1
RETI	4	2		SUB A,(IX/IY+d)	5	3
RETN	4	2		SUB A,A/B/C/D/E/H/L	1	1
RL (HL)	4	2		SUB A, HX/LX/HY/LY	2	2
RL (IX/IY+d)	7	4		SUB A,d	2	2
RL (IX/IY+d),A/B/C/D/E/H/L	7	4		XOR A,(HL)	2	1
RL A/B/C/D/E/H/L	2	2		XOR A,(IX/IY+d)	5	3
RLA	1	1		XOR A,A/B/C/D/E/H/L	1	1
RLC (HL)	4	2		XOR A, HX/LX/HY/LY	2	2
RLC (IX/IY+d)	7	4		XOR A,d	2	2
RLC (IX/IY+d),A/B/C/D/E/H/L	7	4				
RLC A/B/C/D/E/H/L	2	2				
RLCA	1	1		x=[0..7] d=[0..ff]		
RLD	5	2		aa=[0..ffff] a=[0..ff]		
RR (HL)	4	2		m=[0..2]		
RR (IX/IY+d)	7	4		* some exceptions exist		
RR (IX/IY+d),A/B/C/D/E/H/L	7	4				
RR A/B/C/D/E/H/L	2	2				

25 INTERRUPTS

25.1 GENERAL

Interrupts are generated on the CPC by the GATE ARRAY, according to parameters defined by the CRTC. The GATE ARRAY has a counter for this purpose whose objective is to count from 0 to 51 before returning to 0, which is often called **R52**.

This counter is incremented at the end of a HSYNC which is produced according to the parameters defined by the R0, R2 and R3 registers of the CRTC. There is no minimum HSYNC size for R52 to support. It is even if R3=1. However, due to the re-entrance protection mechanism of the HSYNC's, the minimum delay between 2 HSYNC's is 2 μ sec (because it takes at least 1 μ sec between 2 HSYNC's). This implies that the counter can loop in 104 μ sec minimum.

Note that the re-entrance prevention mechanism is bugged on CRTC's from 1 to 4, which allows the creation of an infinite HSYNC depending on the method used (for example R0=R2=0 and R3=1).

In "standard" operation, with a HSYNC programmed every 64 μ sec, 1 interrupt can occur every 3328 μ sec (300 Hz).

On a European standard CPC, this represents 6 interrupts per frame:
6 x 52 lines = 312 lines.

25.2 MANAGEMENT OF R52 COUNTER

There are several particularities of management of the value of counter **R52** by the GATE ARRAY.

It can return to 0:

- When it exceeds 51.
- By setting bit 4 of the MF register of the GATE ARRAY to 1.
- At the end of the 2nd HSYNC after the start of the VSYNC.

Bit 5 of counter R52 changes to 0:

- When an interrupt was armed (pending) and it is authorized while **R52** had continued to evolve.

25.3 TRIGGER CONDITIONS

For an interrupt to occur, it must be triggered.

25.3.1 TRIGGER ON R52=0

The GATE ARRAY sends an interrupt request when R52=0.

- If the interrupts were authorized at the time of the request, then the interrupt takes place and bit 5 of R52 is set to 0 (which is not very useful because it was already equal to 0).
- If interrupts are not authorized, the counter continues to increment, but the interrupt remains armed (the GATE ARRAY then maintains its INT signal). When the interrupt is enabled (via Z80A EI instruction) then:

- An interrupt occurs **after the instruction following the EI**. A HALT following an EI in this circumstance will be considered as 1 NOP.
- Bit 5 of counter R52 is reset to 0 at the "real" end of this instruction. If bit 5 of the counter had reached 1 ($R52 \geq 32$), then this is equal to "removing" 32 rows from the current counter. This has the effect of shifting the moment when the next interrupt can occur.
It prevents less than 20 lines separating 2 interrupts.

25.3.2 TRIGGERING ON VSYNC

Two HSYNC's after the start of VSYNC:

An interrupt is requested by the GATE ARRAY from the Z80A only if bit 5 of R52 is 1. In general, R52 "returns" to 0 when 312 HSYNC's have occurred since the last VSYNC.

But if the screen is not formatted correctly, then the value of R52 may be different from 0.

As described in the previous Chapter, this rudimentary mechanism prevents two interrupts from occurring too closely together.

R52 is set to 0 unconditionally.

25.3.3 Z80A AND INTERRUPTIONS

The Z80A **EI** instruction is used to enable an interrupt to occur as soon as the interrupt is armed. When an interrupt occurs, interrupts are disabled until a new EI occurs. The Z80A's IFF flags are set to 1, which has the same effect as a **DI**.

However, the R52 counter continues to evolve.

If R52 returns to 0, a new interrupt is then pending, and will occur as soon as interrupts are authorized again. Only one interrupt can be pending.

In order to avoid re-entrancy problems in an interrupt code, the designers of the Z80A have imposed that a new interrupt cannot occur on the instruction following the EI.

This was done to allow the **RET**, **RETI**, **RETN** instructions to execute right behind the EI instruction, to prevent the stack from overflowing.

A repetitive sequence of the EI instruction will not allow an interrupt to occur before the end of that sequence, each EI deferring the interrupt.

The Z80A **HALT** instruction is used to wait for an interrupt to occur by repeating NOP's of 1 μ sec indefinitely. If interrupts are not allowed when this instruction is executing, the Z80A will get stuck on this instruction. To my knowledge, few games have used the HALT instruction. However, we can note that the game Trailblazer (published by Gremlin Graphics in 1986) stalls its "split rasters" with a HALT. Indeed, this instruction is interesting insofar as it makes it possible to wedge an interruption to the nearest microsecond.

Indeed, an interrupt cannot cut an instruction (except a repetitive instruction like LDIR or OTIR). So, if the instruction is several microseconds long, the interrupt will occur after the instruction completes.

25.4 INTERRUPT MODE 1

Most code written for the "OLD" AMSTRAD CPC uses the Z80A's IM 1 mode.

We switch to this mode using the **IM 1** instruction.

In this mode, when an interrupt occurs, the code is interrupted with an instruction equivalent to **RST #38**.

The address following the interrupted instruction (or the address of the instruction if it is a repetitive instruction) is put on the stack and PC=#38.

The Z80A RST #38 instruction lasts 4 μ sec when called by code.

When an interrupt occurs, the call in #38 lasts 5 μ sec.

[to test it, just compare the time taken by an RST #38 and the time taken by an interrupt with a fixed time code on 19968 NOP's]

25.5 INTERRUPT MODE 2

IM 2 mode, also called vectorized mode, is designed to allow several peripherals to generate interrupts, via a table of pointers to interrupt routines.

The address of the table is defined, for the most significant address, by the **I register of the Z80A**. The low order byte of the address is normally defined by one of the 128 possible peripherals by indicating its number on the 7 most significant bits, bit 0 equalling 0.

On the "OLD" AMSTRAD CPC, the least significant value of the address is undetermined (High Impedance value) and can vary from one CPC to another.

[I haven't checked if this value can vary while the CPC is on, but the interest in gaining ram is moderate and it's something to avoid]

In the perspective of moving the interrupt address elsewhere than in #38, it is nevertheless possible to use this mode with a few precautions:

It is necessary to create an interrupt vector table containing 257 bytes of the same value.

Indeed, bit 0 of the address of the selected table being unpredictable, this can cause the Z80A to read its vector on the 256th and 257th byte of the table.

If bit 0 is equal to 0, the high and low byte of the vector read from the table will be reversed with respect to a vector read from a table where bit 0 is equal to 1.

It is therefore advisable to create an interrupt vector where the most significant byte of the vector is equal to its less significant byte.

Example: Vector table created in #2000, which contains between #2000 and #2100, 257 times the #CA value. The interrupt then occurring in #CACA (fart!)

The game "*The Great Escape*", published by Ocean Software in 1986, used this mode to free up the first page of 256 bytes. The vector table starts at #100 (I=1) and occupies 257 bytes with the value #BC (for a vector located at #BCBC).

When an interrupt occurs, the call to the pointer located in the table lasts 7 μ sec.

25.6 CRTC & INTERRUPTS...

25.6.1 GENERAL

A HYSYNC begins when the internal condition C0=R2 is met.

Let us recall once again that on CRTC's 0, 1 and 2, the HSYNC visually begins approximately 1 µsec before the display of the corresponding CRTC character.

The display of characters by the GATE ARRAY on these CRTC's starts again from C0 Disp=R2+R3-1 (except for R3=0 for CRTC's 0 and 1).

The measurement of the moment when the interrupt begins is carried out by considering C0vs from the VSYNC signal returned by the PPI.

On CRTC's 3 and 4, the HSYNC begins at the start of the display by the GATE ARRAY of the CRTC character corresponding to C0=R2.

As a general rule, an interrupt always starts 1 µsec after the end of the HSYNC regardless of the CRTC.

Given that the HSYNC starts 1 µsec earlier than expected on a CPC without ASIC (CRTC's 0, 1, 2) there is therefore a delay of 1 µsec with an interruption on a CPC with ASIC (CRTC's 3, 4).

With the same programming of R2 and R3, an interrupt occurs 1 µsec later on CRTC's 3 and 4 than on the other CRTC's, because the ASIC manages a HSYNC synchronous with the display.

HSYNC generated by an ASIC is more compliant with display management.

The following diagrams describe this management according to the CRTC's.

25.6.2 CRTC 0, 1, 2

R3=14	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8 9 10 11 12 13 14														Code interrupted 15 µsec after C0vs=R2																	

R3=8	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8								Code interrupted 9 µsec after C0vs=R2																							

R3=1	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1	Code interrupted 2 µsec after C0vs=R2																														

25.6.3 CRTC 0, 1

R3=0	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			

No interruption

25.6.4 CRTC 2

R3=0	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16																Code interrupted 17 µsec after C0vs=R2															

25.6.5 CRTC 3, 4

R3=14	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8 9 10 11 12 13 14														Code interrupted 16 µsec after C0vs=R2																	

R3=8	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8								Code interrupted 10 µsec after C0vs=R2																							

R3=1	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1	Code interrupted 3 µsec after C0vs=R2																														

R3=0	R2																															
C0 from Vs	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32			
C0 from GA	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31			
C3:	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16																Code interrupted 18 µsec after C0vs=R2															

Note :

Since it is possible to generate "not active" HBLs for the monitor (when $R3 \leq 2$), this implies the possibility of generating interrupts in the visible area.

25.6.6 PERSPECTIVE

The diagram below provides a perspective of a scheduled interrupt under the same conditions according to the different CRTC's.

It should provide an understanding of the mechanisms implemented from the reference C0vs character, considering the different deadlines implemented by the CRTC's.

When it comes to compatibility between the CRTC's, it is therefore necessary to check the differences relating to the delays to consider the registers and the effect of certain values, particularly if these registers are modified when a HSYNC is in progress.

26 CRTC IDENTIFICATION

There are a plethora of methods for identifying a CRTC, most with code, others only visually.

Some methods sometimes involve screen desynchronization and are therefore less well regarded by some purists.

It is also possible to identify a CRTC by being able to identify the machine, as is the case with the CPC+, which has management differences in other circuits (and which have extended functions).

26.1.1 VIA C4 AND/OR C9 OVERFLOW

It is possible to overflow C4 in many different situations depending on the CRTC, whether by programming R0, R9, R4, R7 or even R8.

In general, on CRTC 0, for example, C4 is incremented by default.

In additional management, the value of C4 exceeds the value programmed in R4.

On a CRTC 0, this overrun will occur once.

On CRTC's 1 or 2, this overrun will take place several times depending on the content of R9 and R5.

On CRTC's 3 or 4, there will be no overtaking.

If C4 reaches R7, then a VSYNC may occur.

Example : Screen of 312 lines with R4=36, R9=7, R5=16

$$312 = ((36+1) \times (7+1)) + 16$$

On a CRTC 3 or 4, if R7>36, then the VSYNC does not occur anymore.

On a CRTC 0, if R7>37, then the VSYNC does not occur anymore.

On a CRTC 1 or 2, if R7>39, then the VSYNC does not occur anymore.

26.1.2 VIA VSYNC MANAGEMENT DURING HSYNC

On a CRTC 2, setting R2 and R3 so that VSYNC occurs during the HSYNC period "turns off" VSYNC for the remainder of the C4=R7 period.

It is therefore sufficient to place R2+R3 so that it exceeds the value of R0

26.1.3 VIA CONSIDERATION OF VSYNC ACTIVATION

When the VSYNC is triggered by positioning R7 with C4, when C0>0, the line counter of the VSYNC is different according to the CRTC's. It starts from 0 on a CRTC 0, and from 1 on a CRTC 1, while no VSYNC occurs in this condition on a CRTC's 3 or 4.

26.1.4 VIA VSYNC LENGTH

Only CRTC's 0, 3 and 4 can manage the length of the VSYNC.

A VSYNC on CRTC's 1 and 2, which starts when R7 was programmed before C4=R7, lasts 16 lines.

26.1.5 VIA HSYNC LENGTH

On CRTC's 2, 3 and 4, the HSYNC lasts 16 µsec when R3=0.

On CRTC's 0 and 1, there is no HSYNC when R3=0.

There is therefore no interruption, which is one of the methods for testing the consequences of the value 0 on R3.

26.1.6 VIA THE BORDER, VISUALY

- a) CRTC 2 whose C0=0 during the HSYNC can no longer deactivate its BORDER.
- b) CRTC's 0 and 2, of which R6=0 is in conflict when C4=C9=0, alternates background and BORDER bytes (at least on the first line without adequate programming).
- c) CRTC's 0 and 2 will create a BORDER byte when C0 reaches R0 (and R1>R0).
- d) CRTC's 0, 3 and 4 can deactivate the BORDER (or add delays on taking the BORDER into account) with the SKEW BIT function of R8, whereas this function does not exist on CRTC's 1 and 2.

26.1.7 VIA THE INTERLACE MODE

C4 counting methods are different depending on the CRTC.

On CRTC 2, the count of C4 is not affected.

Being the only one, it is therefore detectable once the others have been identified.

On CRTC's 0 and 1, with R9 programmed respectively with 6 and 7 without having modified R7, the VSYNC occurs 2 times faster, since C4=R7 with characters of 4 lines instead of 8.

26.1.8 VIA STATUS REGISTER &BE00

Only on CRTC 1, is it possible to test the transition of bit 6 at the appropriate time.

On CRTC's 3 and 4, the port at &BE00 behaves like the one at &BF00 (see below)

26.1.9 VIA READ REGISTER &BF00

On CRTC 0, it is possible to read R12 and R13, as well as R14/R15 (cursor) and R15/R17 (light pen). The register number value is truncated to 5 bits. Thus, selecting register 108 is equivalent to selecting register 12.

On CRTC 1, this register returns 0 on all registers, except for register 31 (and all registers whose bits 0 to 4 are at 1). Values 255 and 127 were observed.

On CRTC 2, this register is used to read registers R16 and R17. The value 0 is returned on all other register numbers. The register number value is truncated to 5 bits.

On CRTC's 3 and 4, it is possible to read registers R12, R13, R16 and R17. However, the register number read comes from a table of 8 registers on 3 bits. Reading R4 or R20 is equivalent to reading R12.

On CRTC's 3 and 4, reading R10 and R11 (or equivalent for the first 3 bits) returns values internal to the ASIC (see dedicated Chapter).

26.1.10 VIA R10/R11 STATUS REGISTERS

Only on CRTC's 3 and 4, it is possible to test the update of many bits at the appropriate time, such as for example bit 0 of status 1 which is worth 1 when C0=R0 (0 otherwise). Furthermore (and subject to additional tests), bit 3 of status 2 should allow to differentiate between CRTC 3 and CRTC 4.

27 CPC IDENTIFICATION

It is possible to identify CPC models from differences which are not related to the CRTC or ROM content.

This is the case for the 2 machines which have ASIC's:

CPC PLUS ASIC 40489 CRTC 3

CPC LOWCOST ASIC 40226 CRTC 4

27.1 IDENTIFICATION METHODS

27.1.1 ENABLING EXTENDED FEATURES

CPC PLUS : Activation via an unlock sequence sent to the CRTC.

CPC LOWCOST : No extended functions (without the secret sequence).

OTHER CPCs : No extended functions.

27.1.2 BUG PPI PORT C

CPC PLUS : When the command register is used to configure port C, the bits of this port are reset to 0. The ASIC poorly emulates the PPI and does not reset these bits to 0. Very annoying for the compatibility of keyboard routines between the CPC PLUS and older models.

CPC LOWCOST: The 8255 PPI is not emulated by the 40226 ASIC. These CPC's have a PPI and therefore behave like the first generation of CPC's.

OTHER CPCs: Port C bits are normally zeroed by the command register.

27.1.3 BUG PPI PORT B

On a PPI, you can program the direction of port B (input or output).

At the output, we can therefore place a value there, which we can read again.

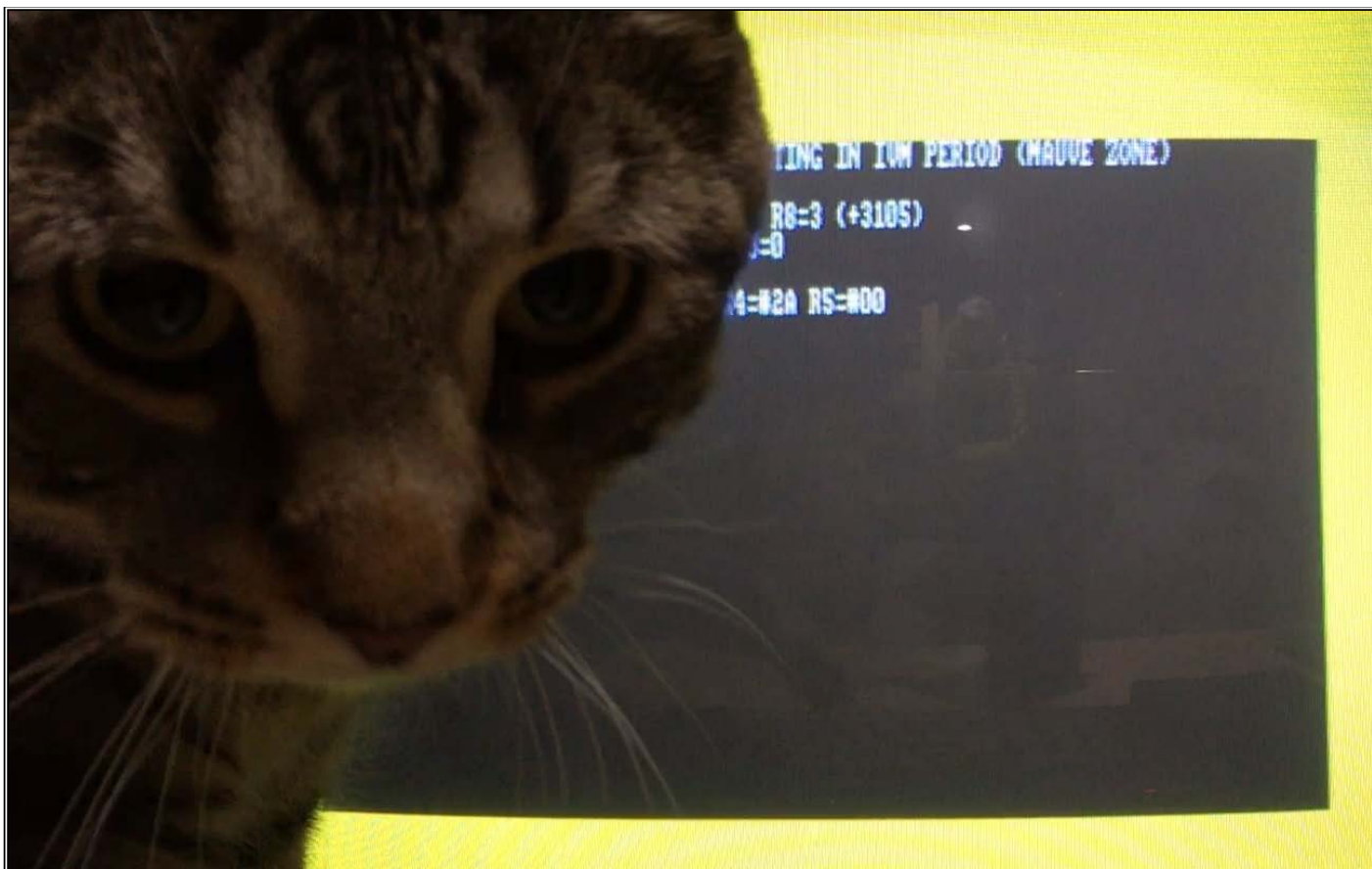
The PPI of CPC LOWCOST would not make it possible to read back a value stored in the port B placed in output. We therefore systematically read the value of port B as input (and therefore the peripherals connected to it). This remains to be verified however, failing to indicate which PPIs were installed in the test CPC's.

AMSTRAD used, as per the case for CRTC's, 8255 PPIs from several different manufacturers.

We can count the following circuits, used in all models without distinction (464, 664, 6128)

- NEC D8255AC-2
- NEC D8255AC-5
- TOSHIBA TMP8255AP-5

Note that the difference between "-2" and "-5" is due to the maximum frequency manageable by the circuit (4 MHz for the "-5" and 5 MHz for the "-2")



Raaahhhhhhhh !!
Idiot Canadian Cat Curious in front of a CPC

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