AMSTRAD CPC / CRTC 2

SHAKER V1.9 OUTPUT

LOGON SYSTEM 2021 / LONGSHOT

More information about CRTC in Amstrad Cpc Crtc Compendium
(“con de chat canadien”)

Sommaire

UPDATE VRAM VS CRTC

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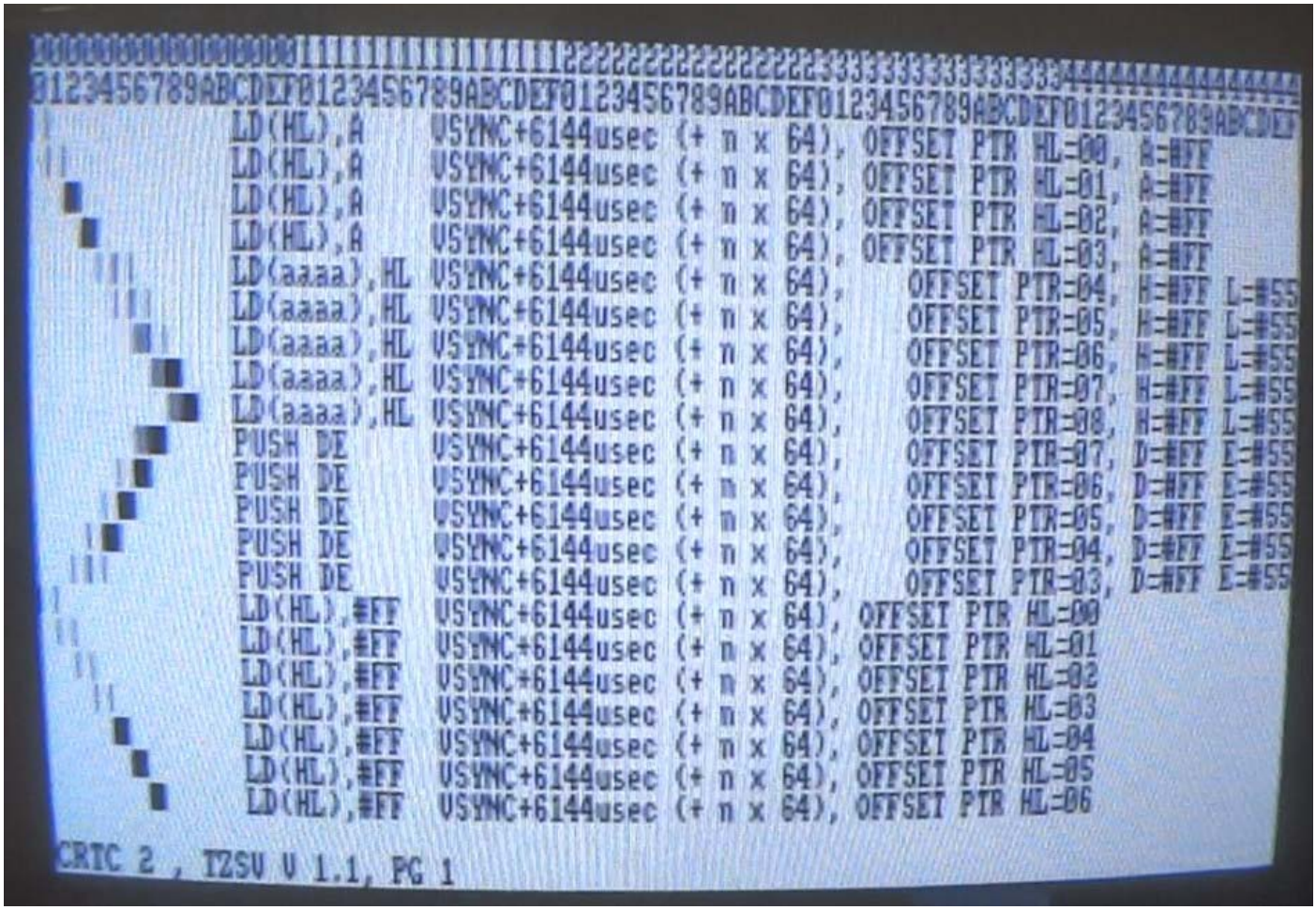
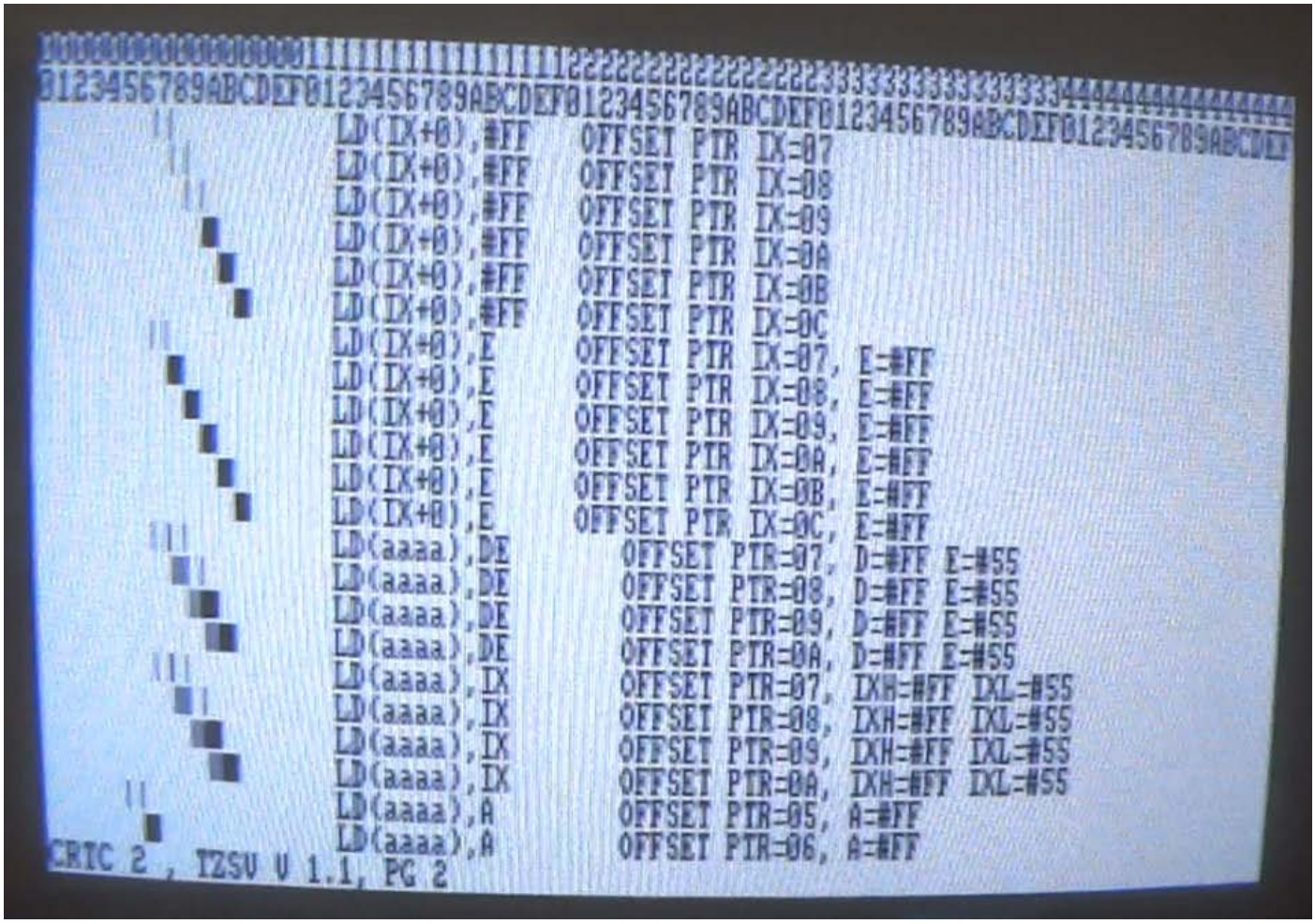
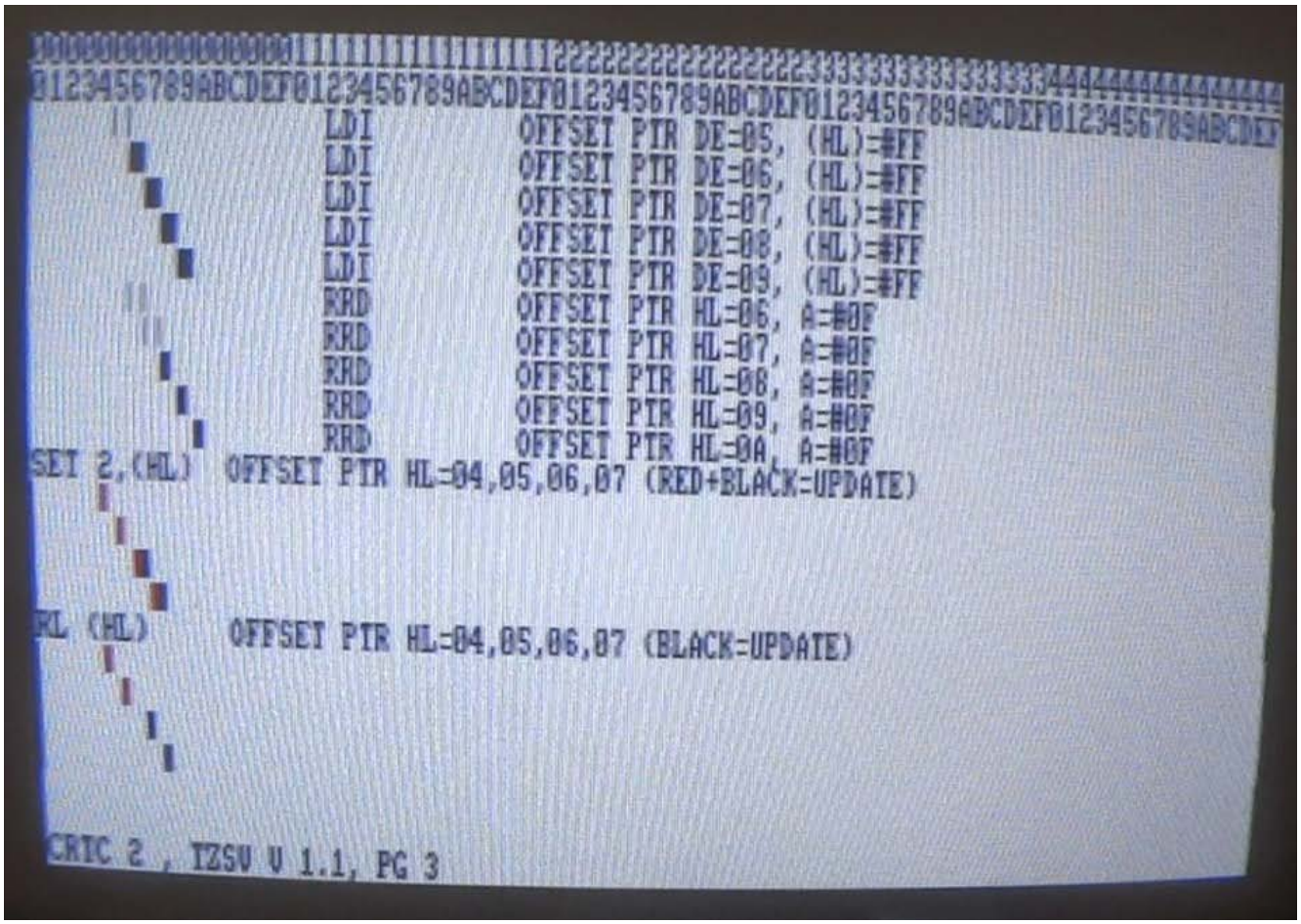
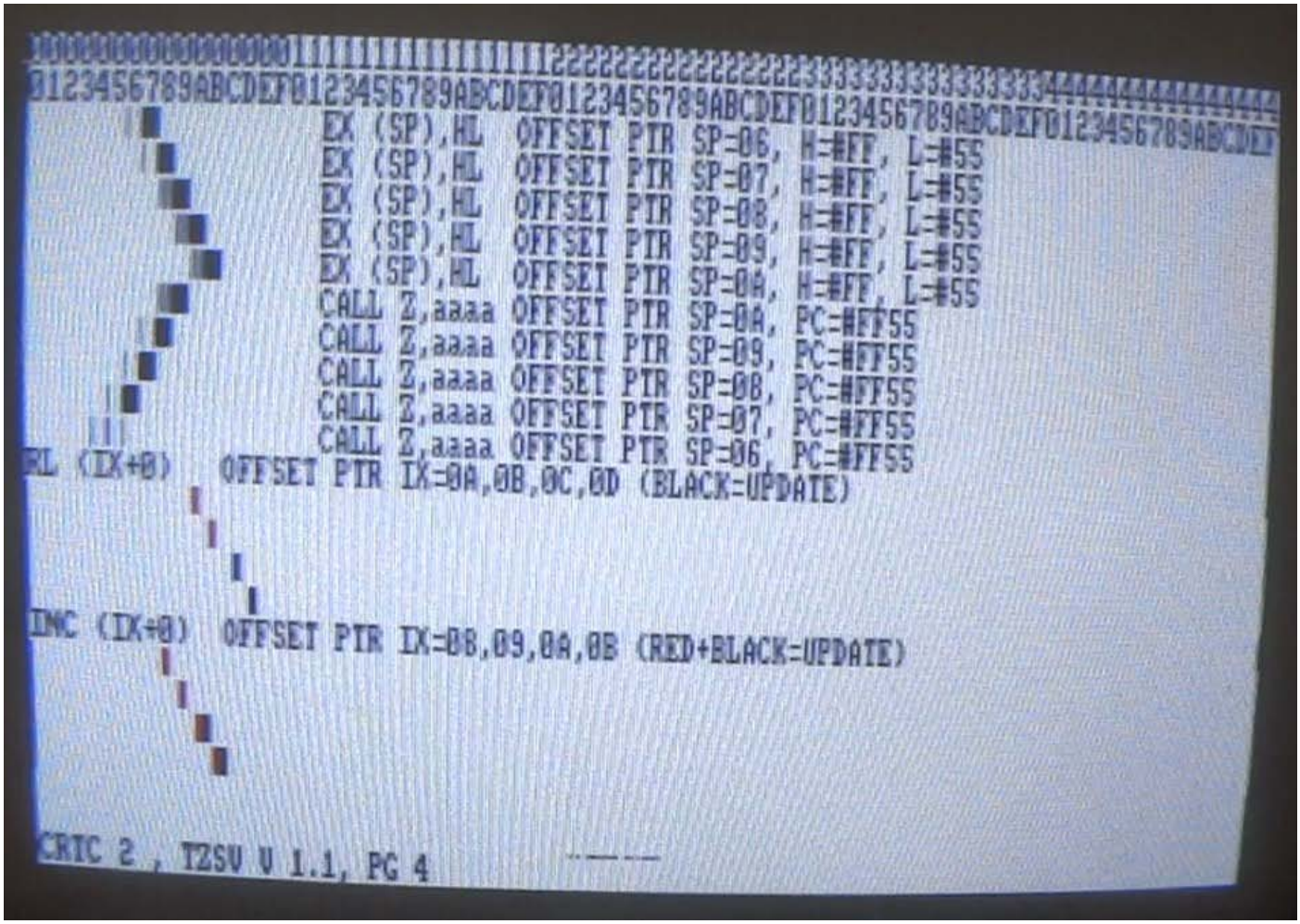
CPC SHAKER 1.9 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (79 TST)                    (F9) MODULE 1
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(0) CRTC 2 RUMB
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```




LD(IX+0),#FF OFFSET PTR IX=07
LD(IX+0),#FF OFFSET PTR IX=08
LD(IX+0),#FF OFFSET PTR IX=09
LD(IX+0),#FF OFFSET PTR IX=0A
LD(IX+0),#FF OFFSET PTR IX=0B
LD(IX+0),#FF OFFSET PTR IX=0C
LD(IX+0),E OFFSET PTR IX=07, E=#FF
LD(IX+0),E OFFSET PTR IX=08, E=#FF
LD(IX+0),E OFFSET PTR IX=09, E=#FF
LD(IX+0),E OFFSET PTR IX=0A, E=#FF
LD(IX+0),E OFFSET PTR IX=0B, E=#FF
LD(IX+0),E OFFSET PTR IX=0C, E=#FF
LD(aaaa),DE OFFSET PTR=07, D=#FF E=#55
LD(aaaa),DE OFFSET PTR=08, D=#FF E=#55
LD(aaaa),DE OFFSET PTR=09, D=#FF E=#55
LD(aaaa),DE OFFSET PTR=0A, D=#FF E=#55
LD(aaaa),IX OFFSET PTR=07, IXH=#FF IXL=#55
LD(aaaa),IX OFFSET PTR=08, IXH=#FF IXL=#55
LD(aaaa),IX OFFSET PTR=09, IXH=#FF IXL=#55
LD(aaaa),IX OFFSET PTR=0A, IXH=#FF IXL=#55
LD(aaaa),A OFFSET PTR=05, A=#FF
LD(aaaa),A OFFSET PTR=06, A=#FF
CRTC 2 , TZSV V 1.1, PG 2

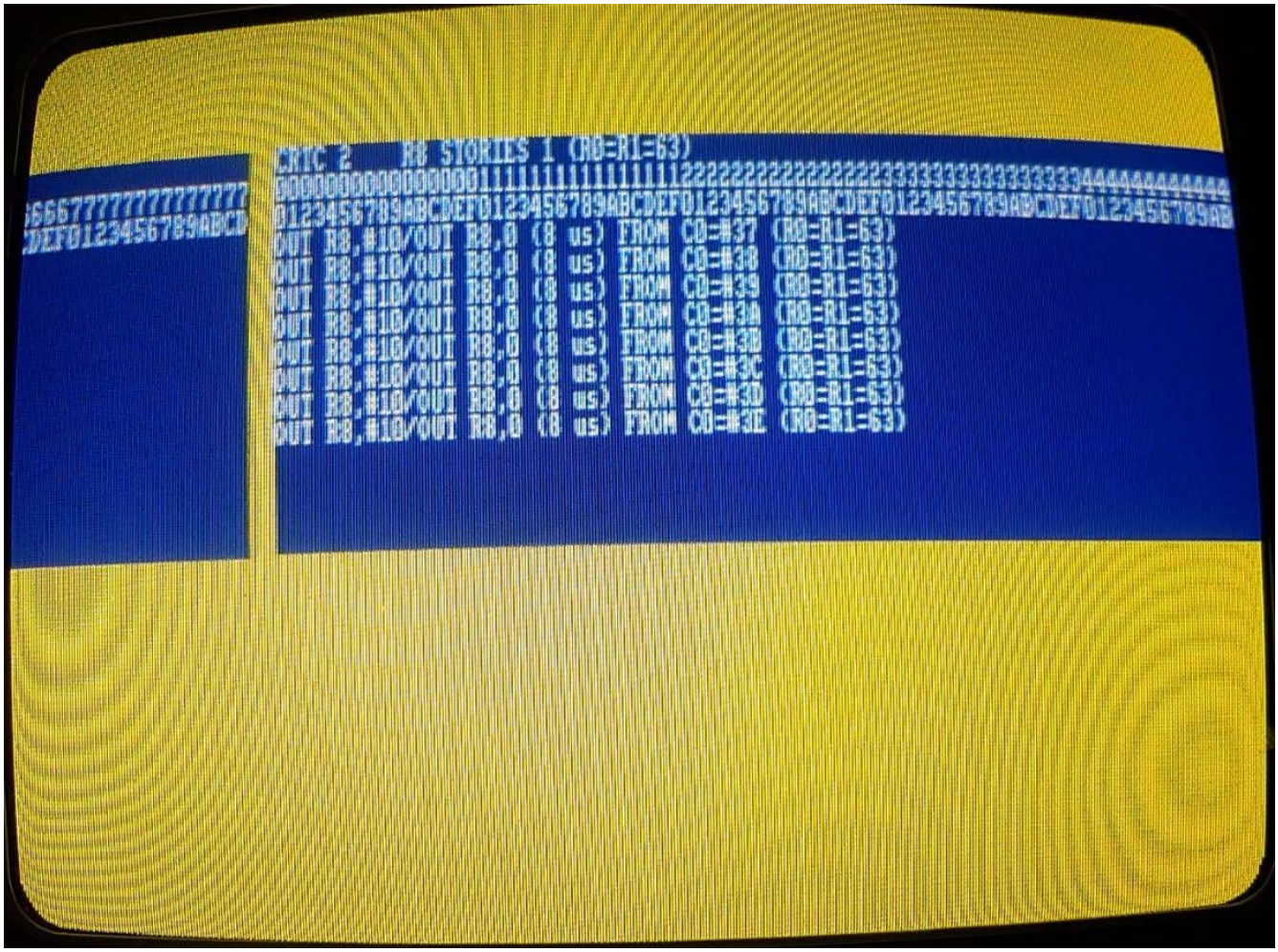

LDI OFFSET PTR DE=05, (HL)=#FF
LDI OFFSET PTR DE=06, (HL)=#FF
LDI OFFSET PTR DE=07, (HL)=#FF
LDI OFFSET PTR DE=08, (HL)=#FF
LDI OFFSET PTR DE=09, (HL)=#FF
RRD OFFSET PTR HL=06, A=#0F
RRD OFFSET PTR HL=07, A=#0F
RRD OFFSET PTR HL=08, A=#0F
RRD OFFSET PTR HL=09, A=#0F
RRD OFFSET PTR HL=0A, A=#0F
SET 2,(HL) OFFSET PTR HL=04,05,06,07 (RED+BLACK=UPDATE)
RL (HL) OFFSET PTR HL=04,05,06,07 (BLACK=UPDATE)
CRTC 2 , TZSV V 1.1, PG 3

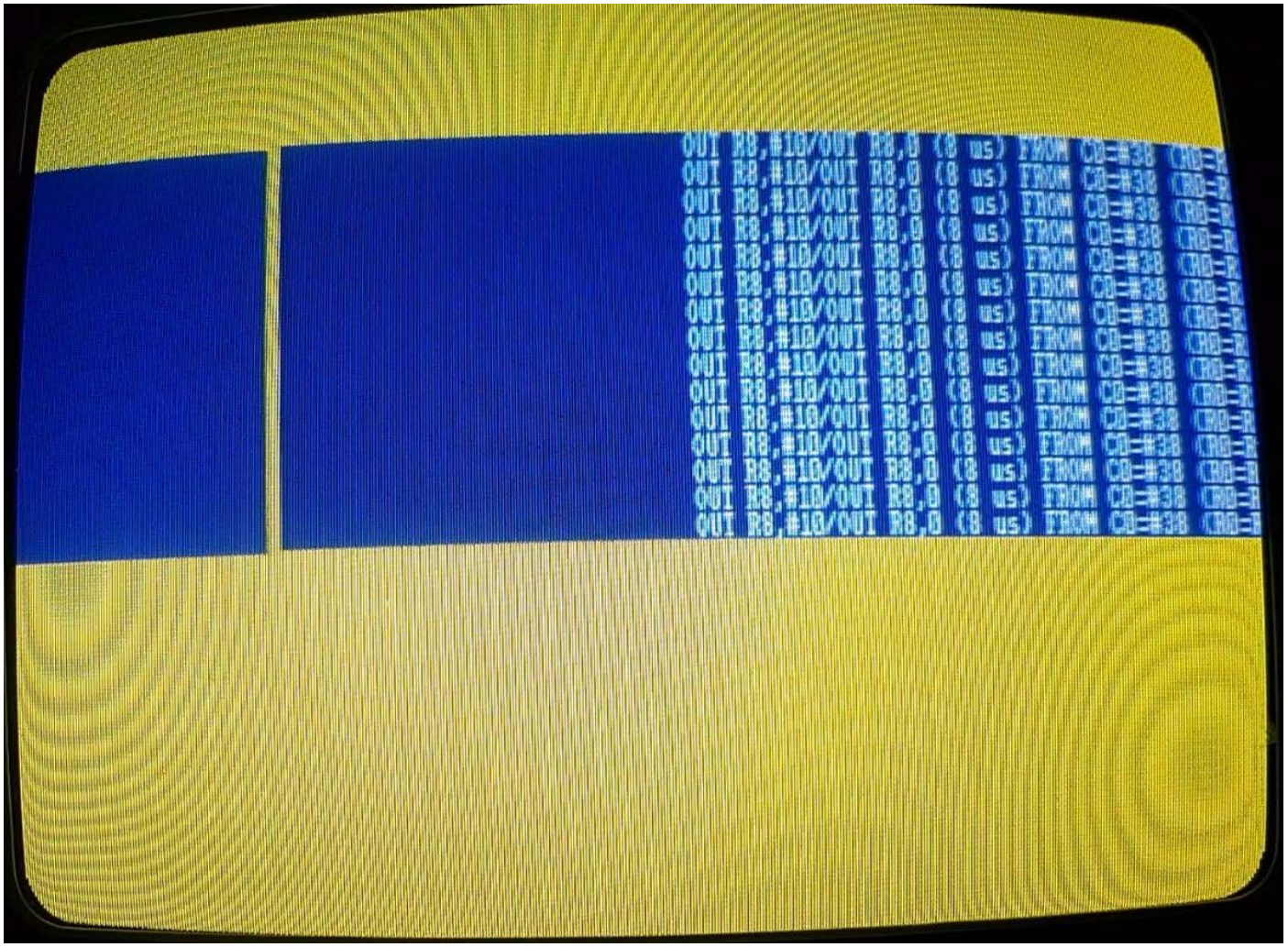


Note : WinApe 2.0 Beta 3 wrong on LDI (page 3) and EX(SP),HL (page 4) (Ok with others instrutions)

SKEW DISP ON R0 RUPTURE

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```




OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38
OUT R8,#10/OUT R8,0 (8 us) FROM C0=#38

INTERRUPT DELAY FROM R2

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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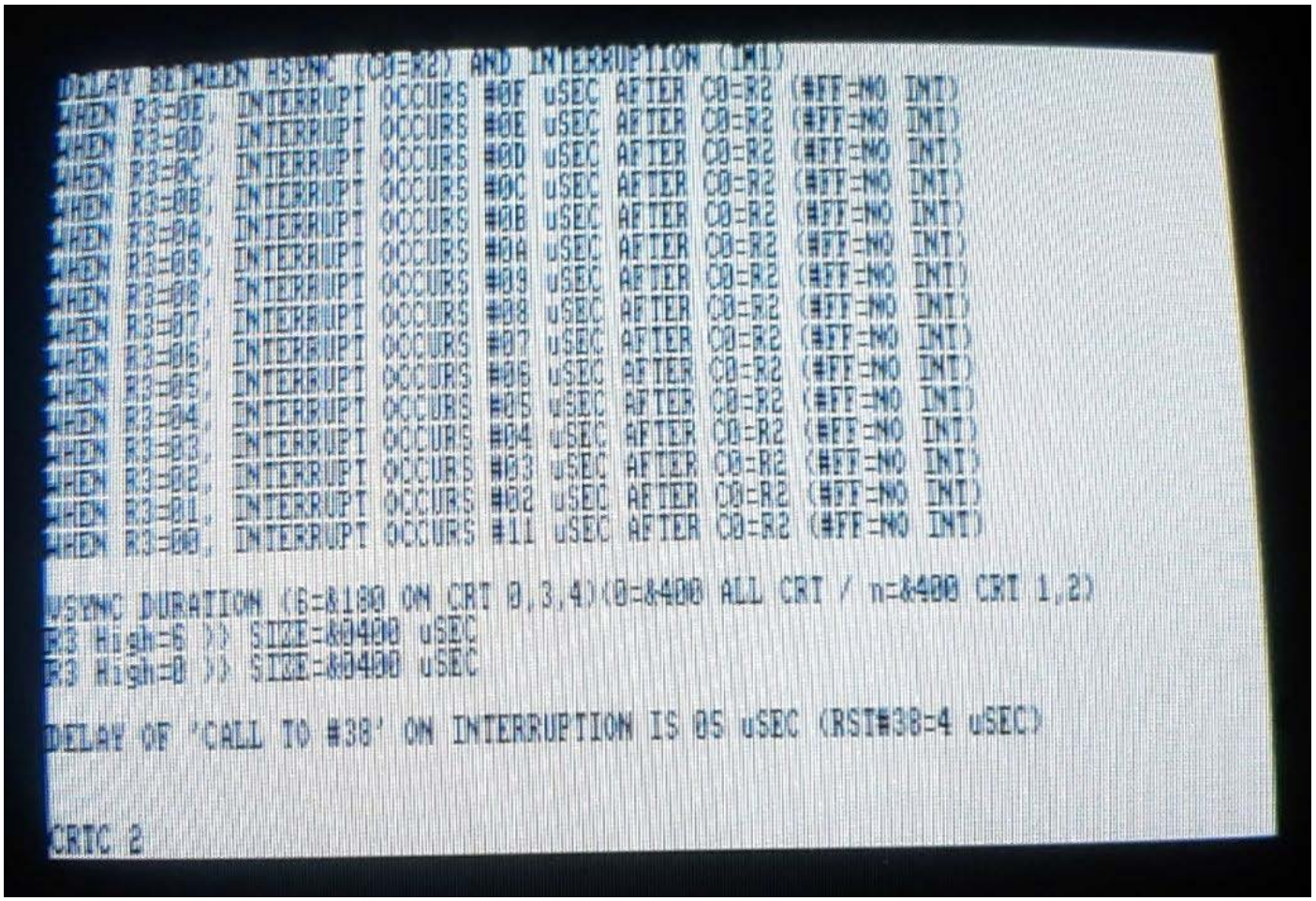

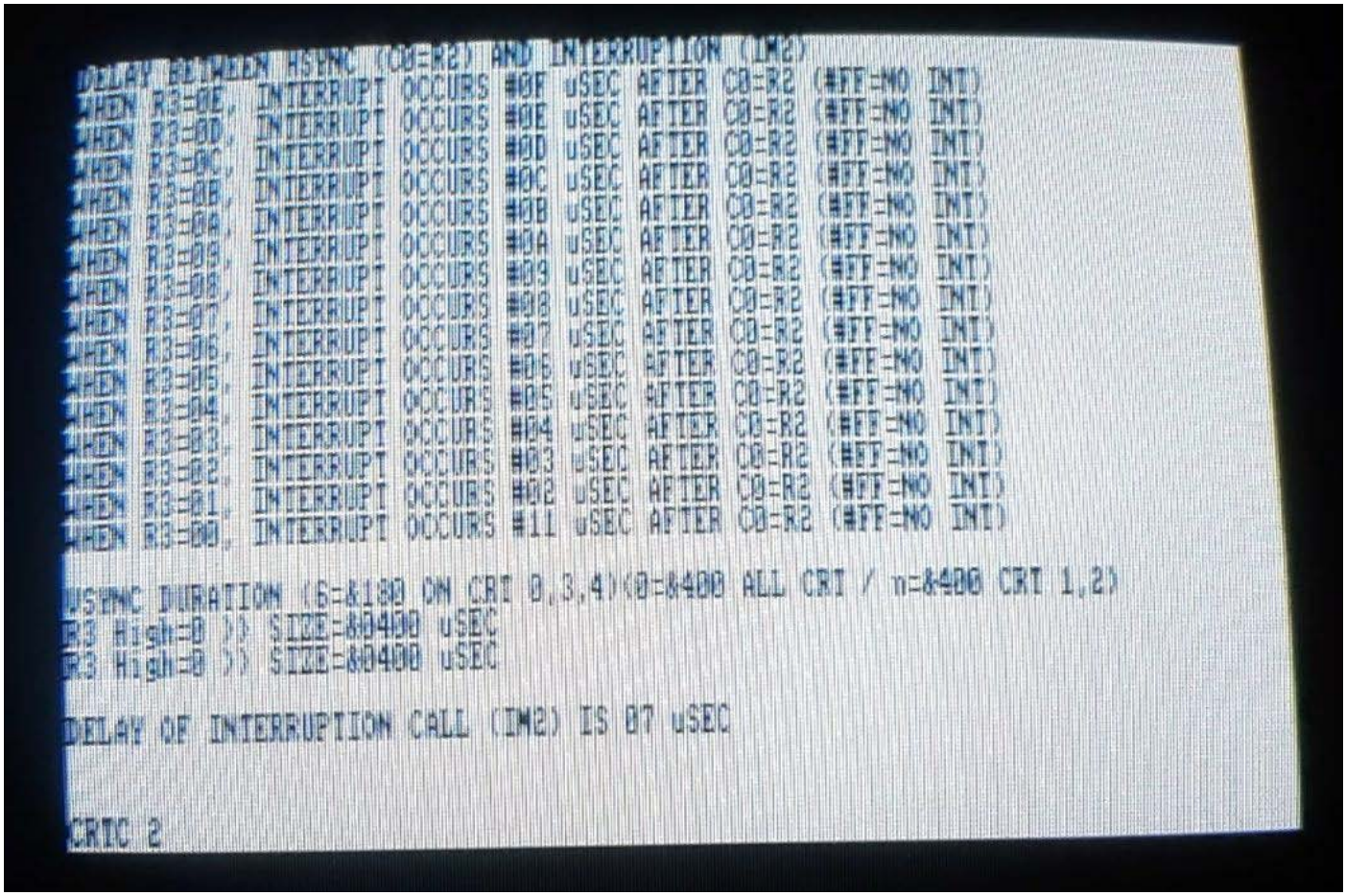
DELAY BETWEEN HSYNC (C0=R2) AND INTERRUPTION (IM2)
WHEN R3=0E, INTERRUPT OCCURS #0F uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=0D, INTERRUPT OCCURS #0E uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=0C, INTERRUPT OCCURS #0D uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=0B, INTERRUPT OCCURS #0C uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=0A, INTERRUPT OCCURS #0B uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=09, INTERRUPT OCCURS #0A uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=08, INTERRUPT OCCURS #09 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=07, INTERRUPT OCCURS #08 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=06, INTERRUPT OCCURS #07 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=05, INTERRUPT OCCURS #06 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=04, INTERRUPT OCCURS #05 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=03, INTERRUPT OCCURS #04 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=02, INTERRUPT OCCURS #03 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=01, INTERRUPT OCCURS #02 uSEC AFTER C0=R2 (#FF=NO INT)
WHEN R3=00, INTERRUPT OCCURS #11 uSEC AFTER C0=R2 (#FF=NO INT)
HSYNC DURATION (6=&180 ON CRT 0,3,4)(0=&400 ALL CRT / n=&400 CRT 1,2)
R3 High=0)) SIZE=&0400 uSEC
R3 High=0)) SIZE=&0400 uSEC
DELAY OF INTERRUPTION CALL (IM2) IS 07 uSEC
CRTC 2

UPDATE CRTC R0 TIMING

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
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(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
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(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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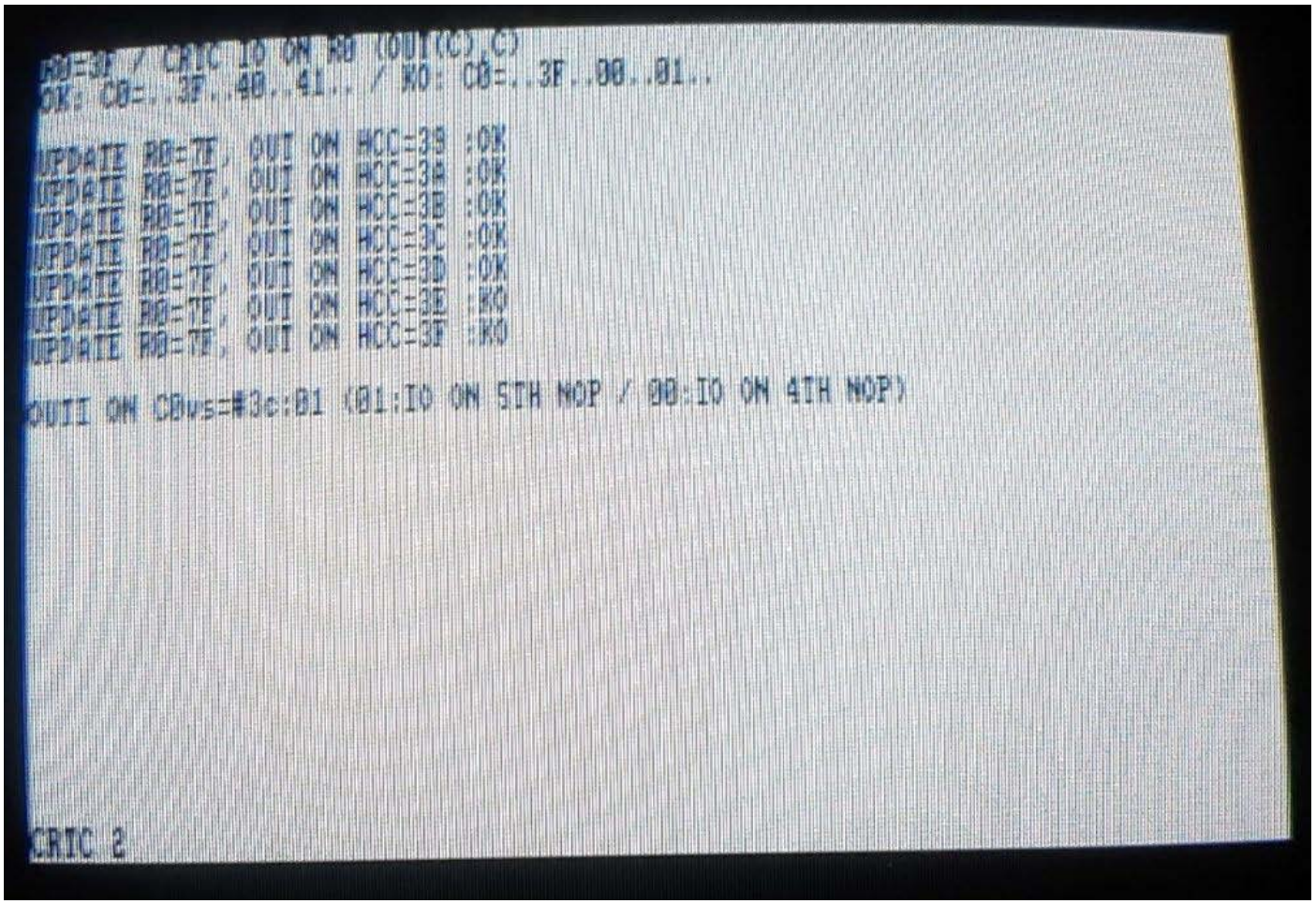
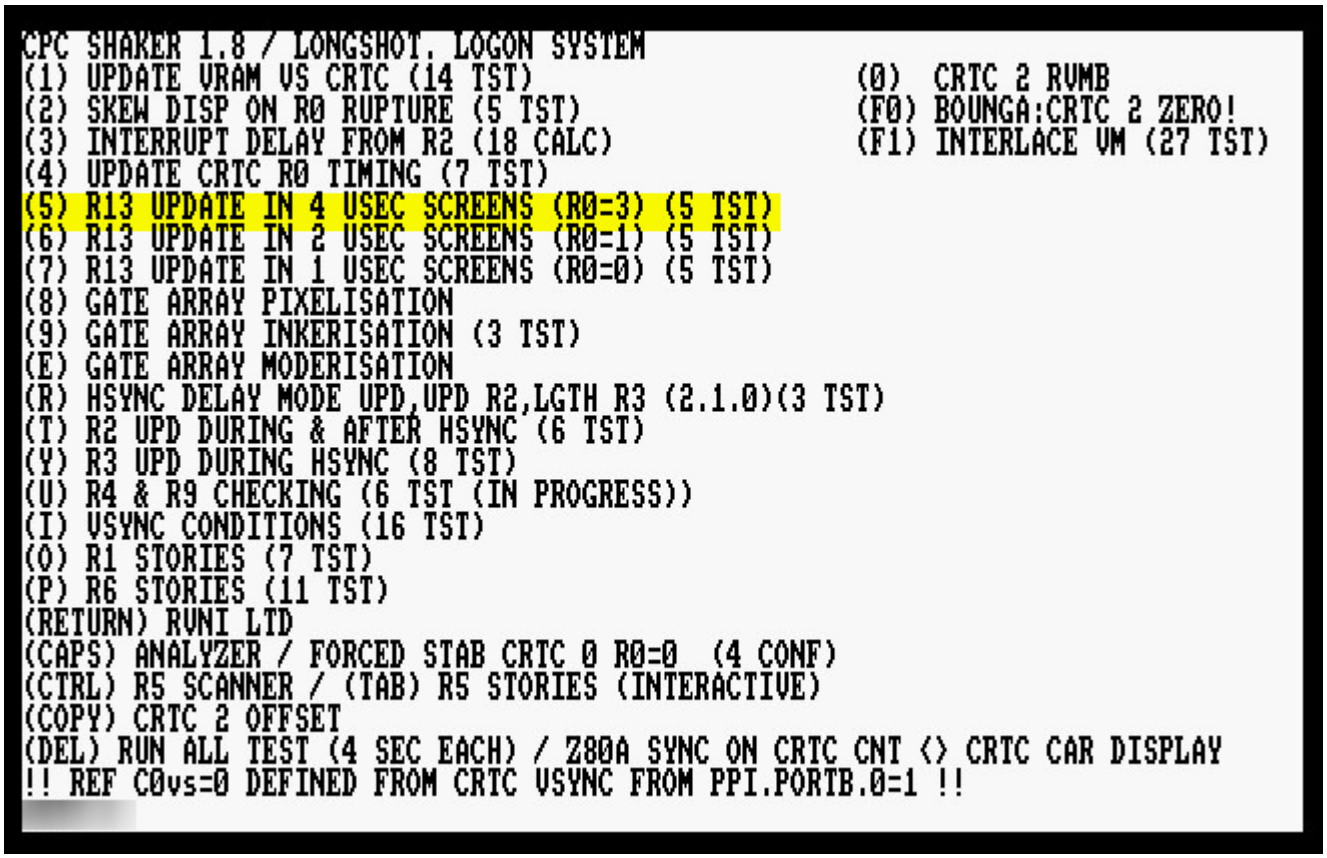
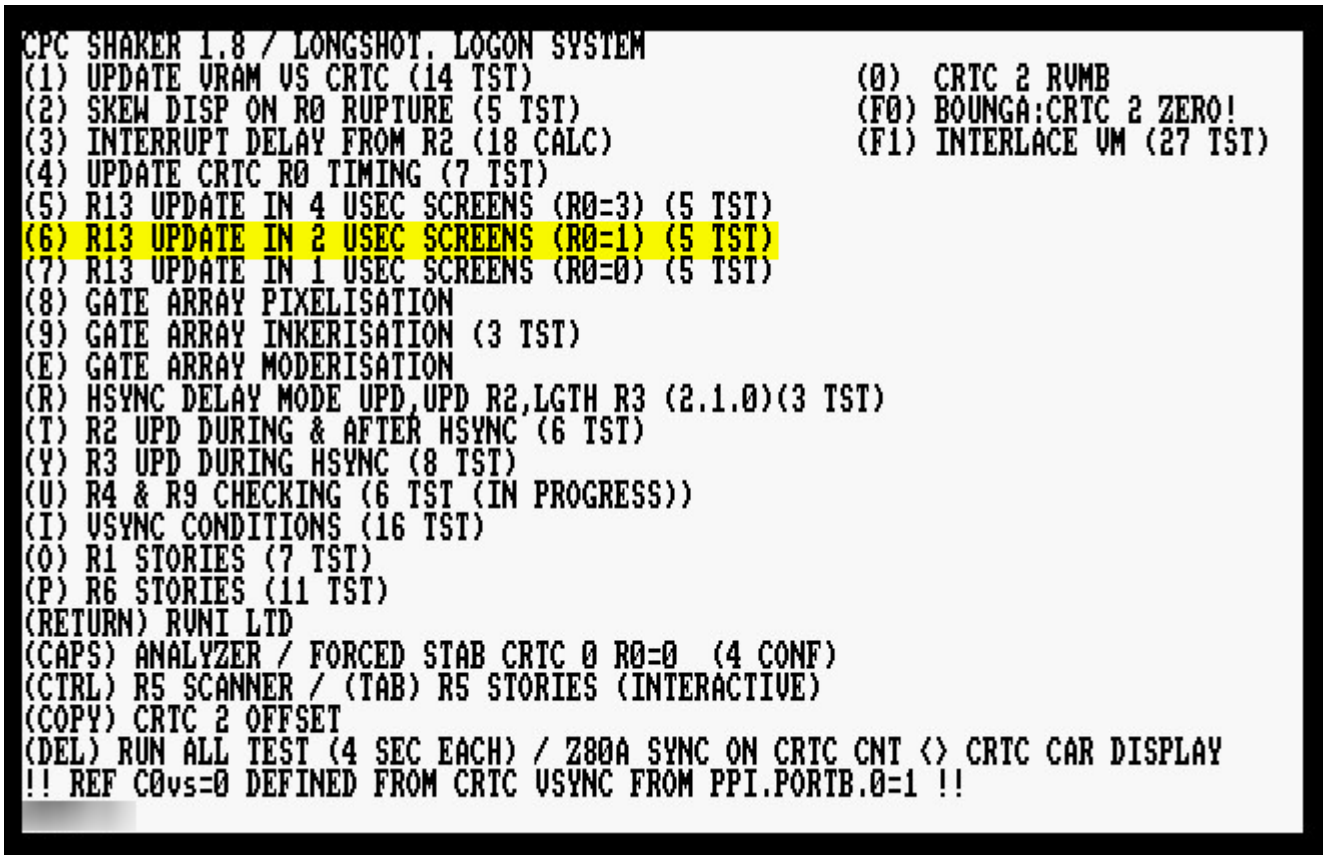


R13 UPDATE IN 4 USEC SCREENS (R0=3)



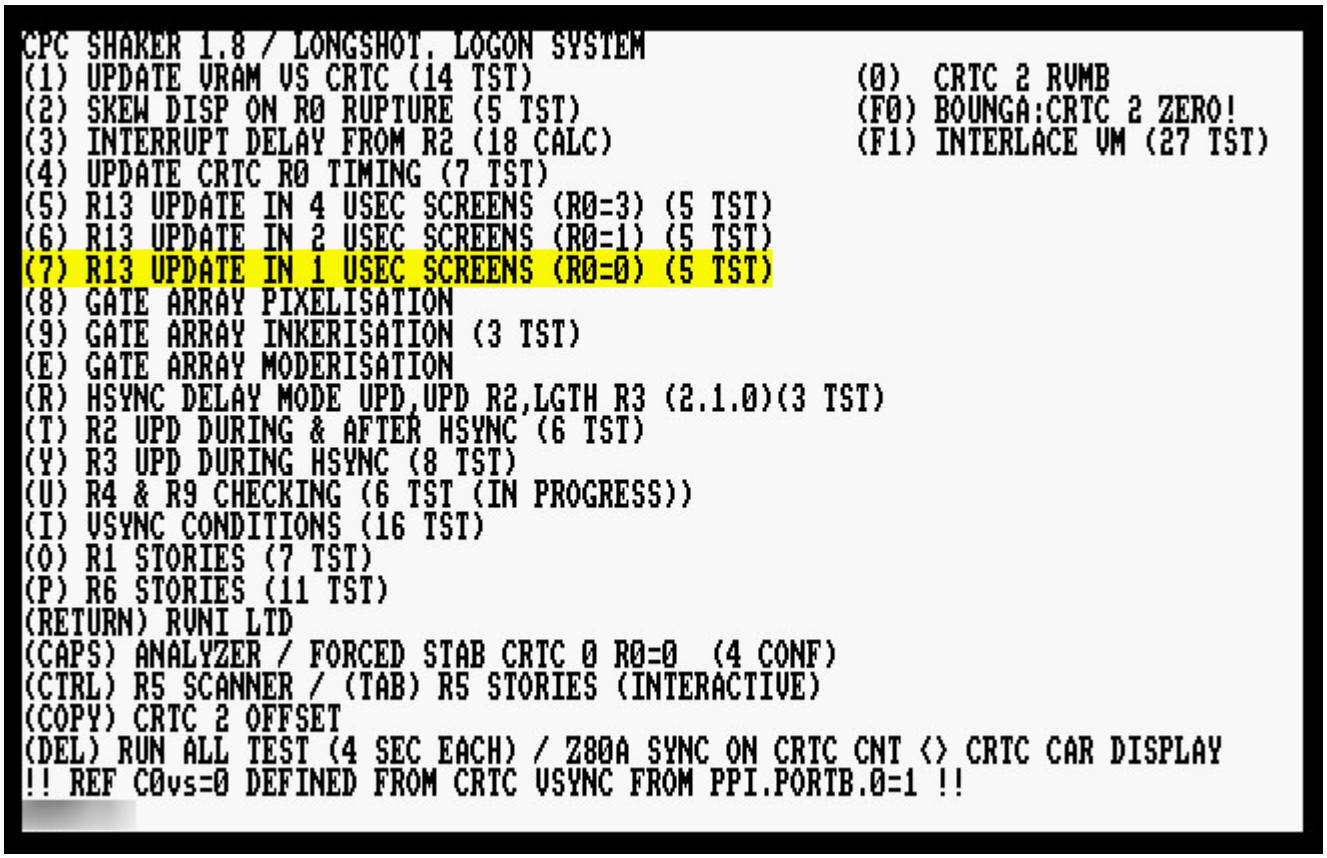
Not available on CRTC 2

R13 UPDATE IN 2 USEC SCREENS (R0=1)



Not available on CRTC 2

R13 UPDATE IN 1 USEC SCREENS (R0=0)



Not available on CRTC 2

GATE ARRAY PIXELISATION

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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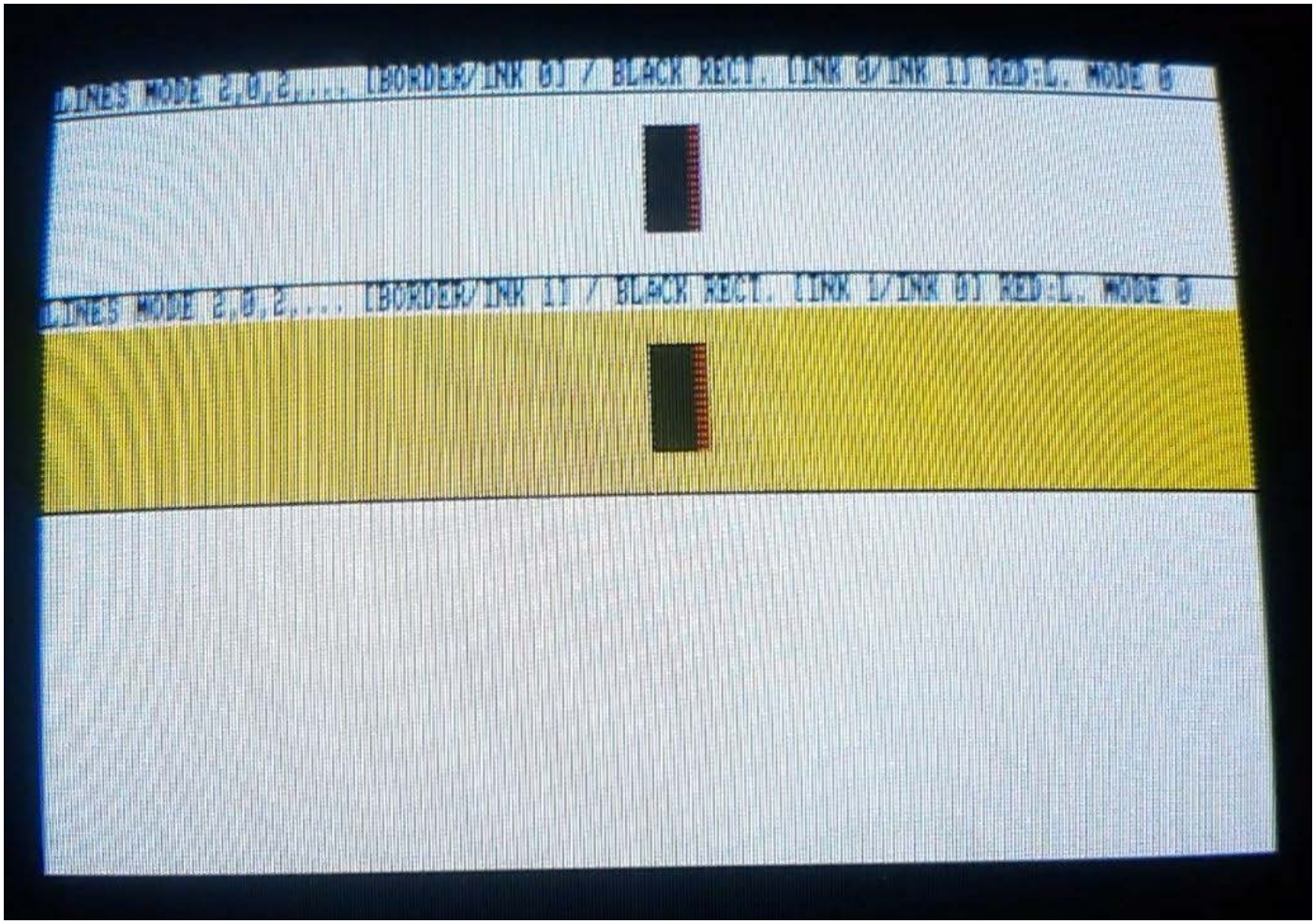

GATE ARRAY INKERISATION

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
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(I) VSYNC CONDITIONS (16 TST)
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(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
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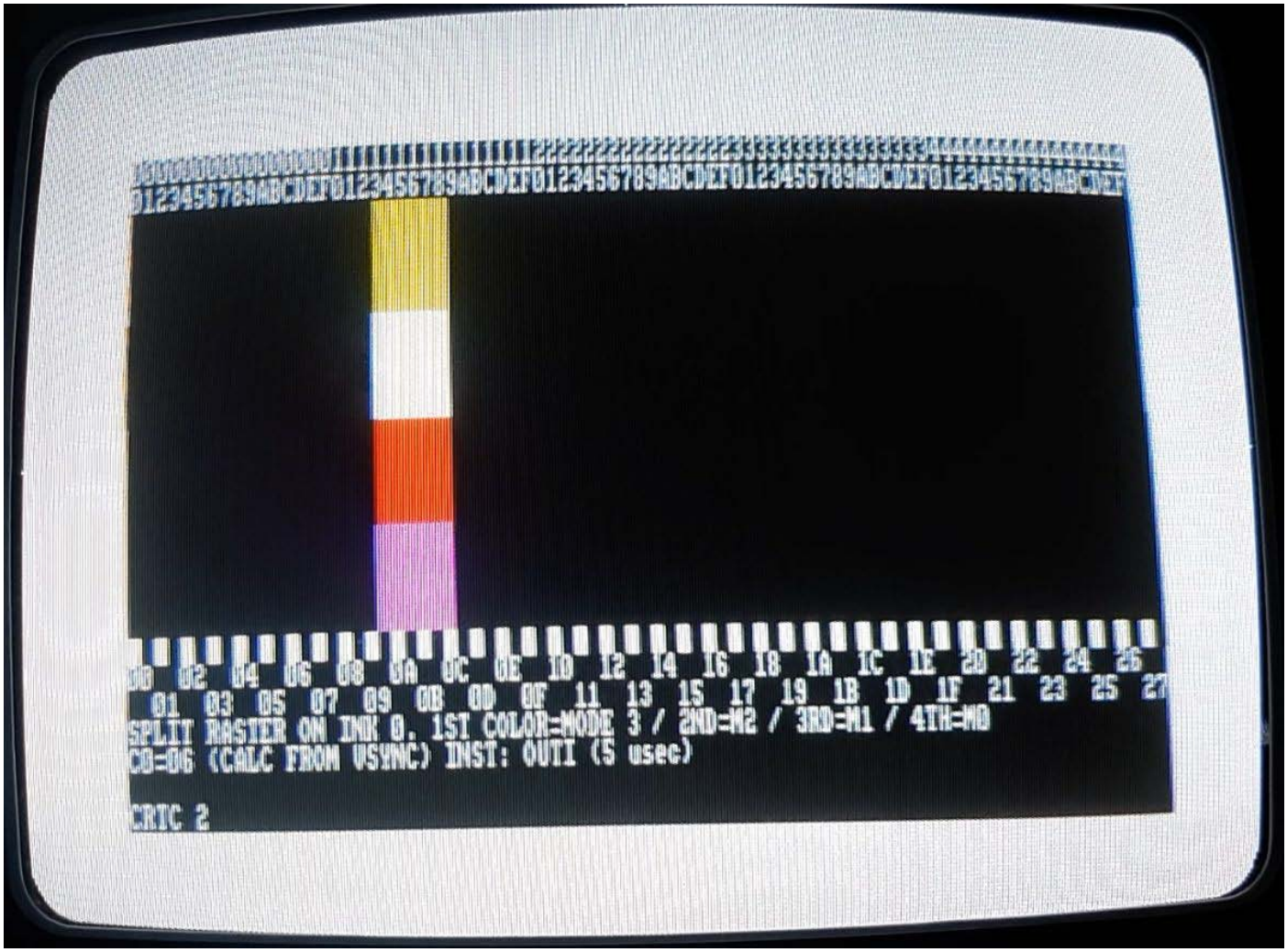
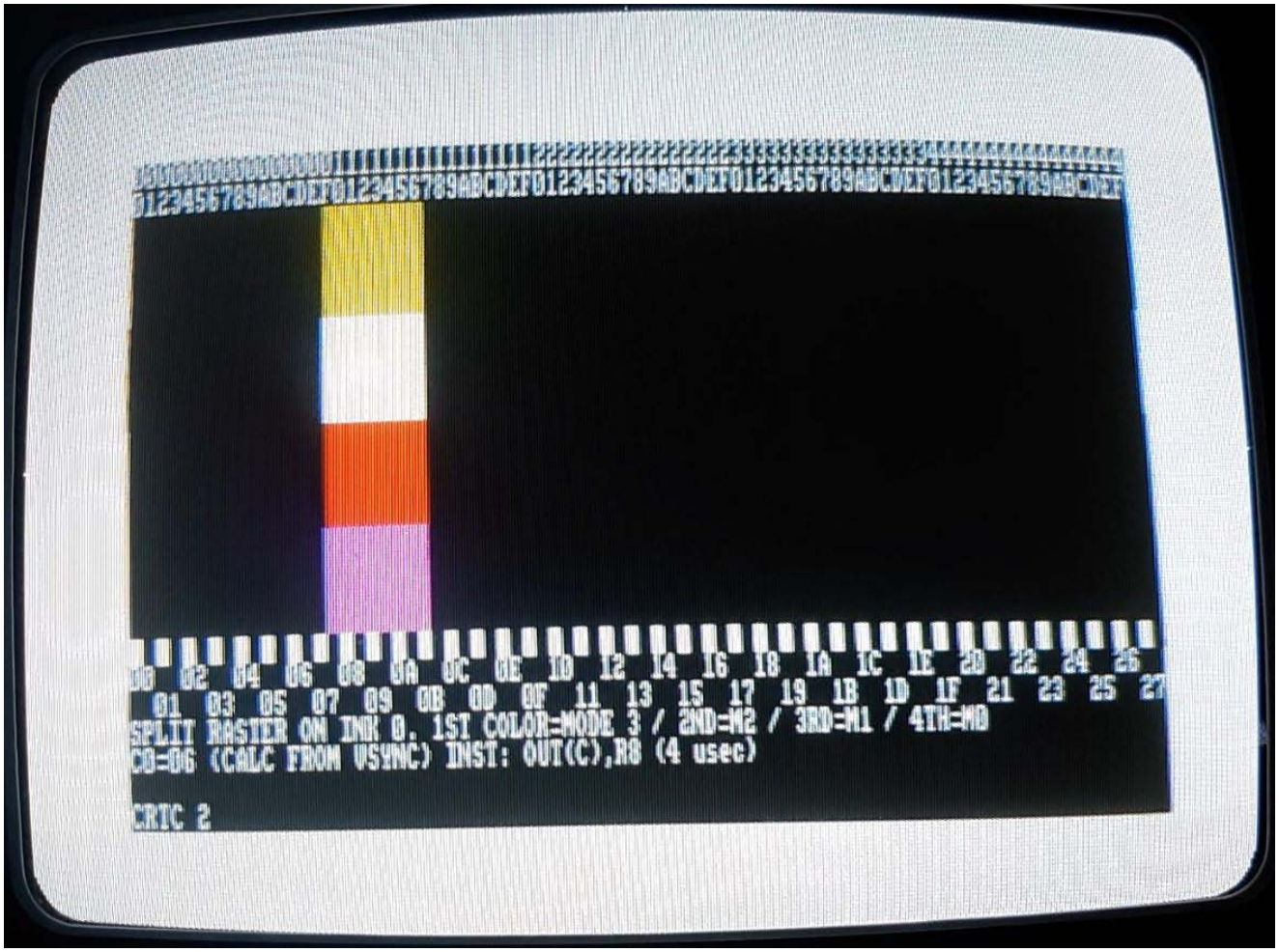
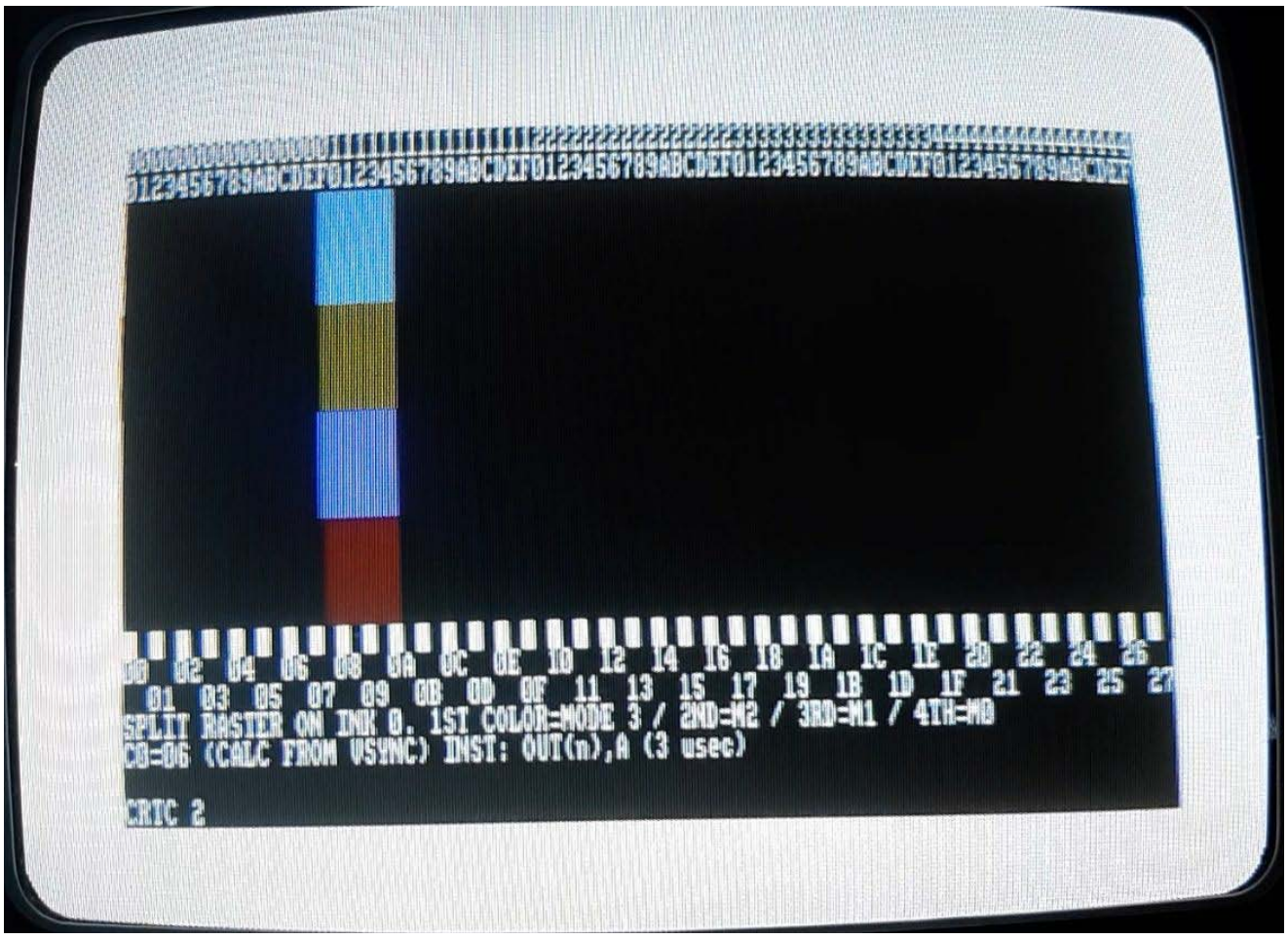



SPLIT RASTER ON INK 0. 1ST COLOR=MODE 3 / 2ND=M2 / 3RD=M1 / 4TH=M0
C0=06 (CALC FROM VSYNC) INST: OUT(C),R0 (4 usec)
CRTC 2


SPLIT RASTER ON INK 0. 1ST COLOR=MODE 3 / 2ND=M2 / 3RD=M1 / 4TH=M0
C0=06 (CALC FROM VSYNC) INST: OUT(n),A (3 usec)
CRTC 2

GATE ARRAY MODERISATION

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
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(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
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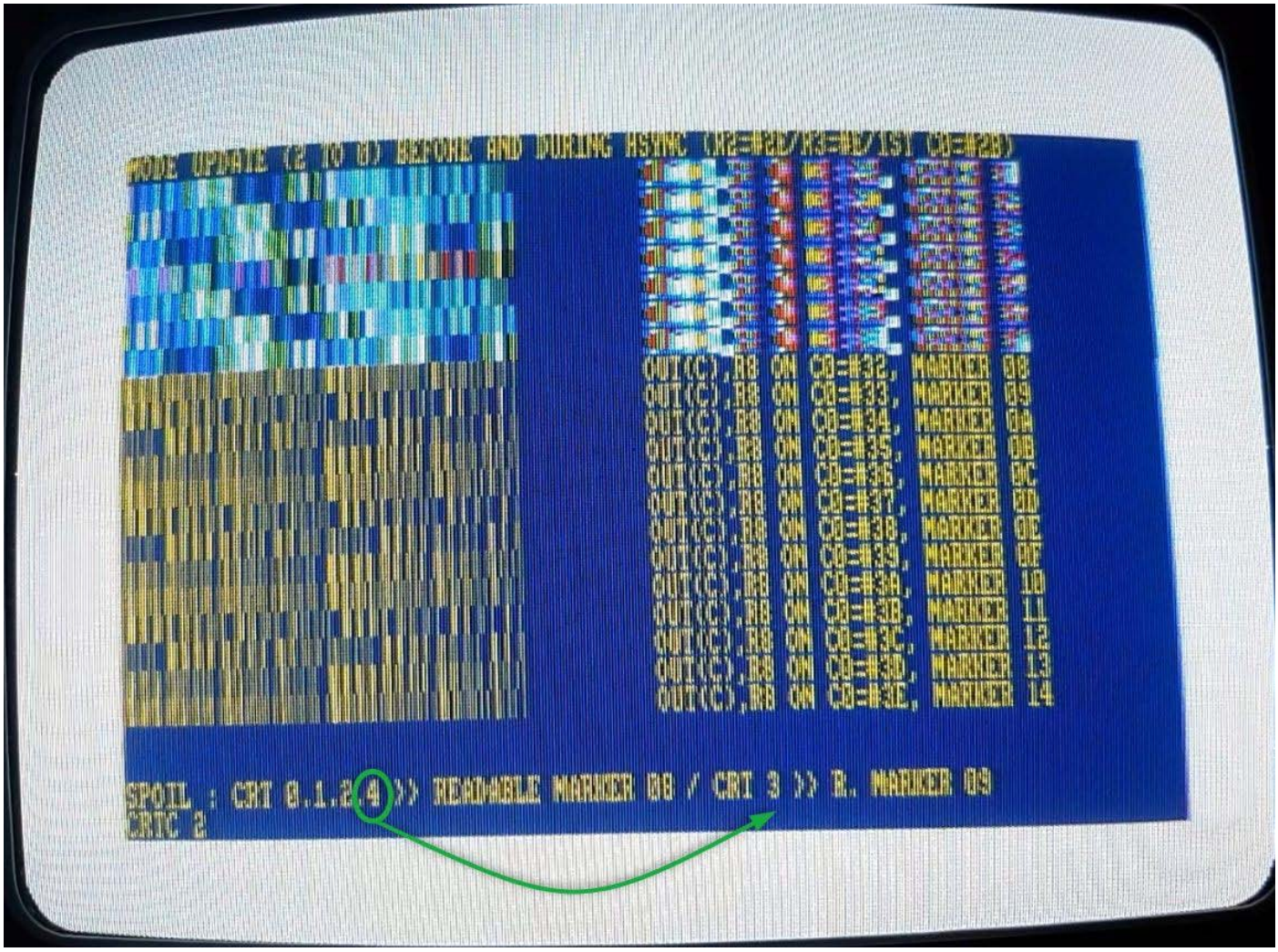

HSYNC DELAY ON MODE UPDATE, R2 UPDATE/R3 LENGTH 2 to 0

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
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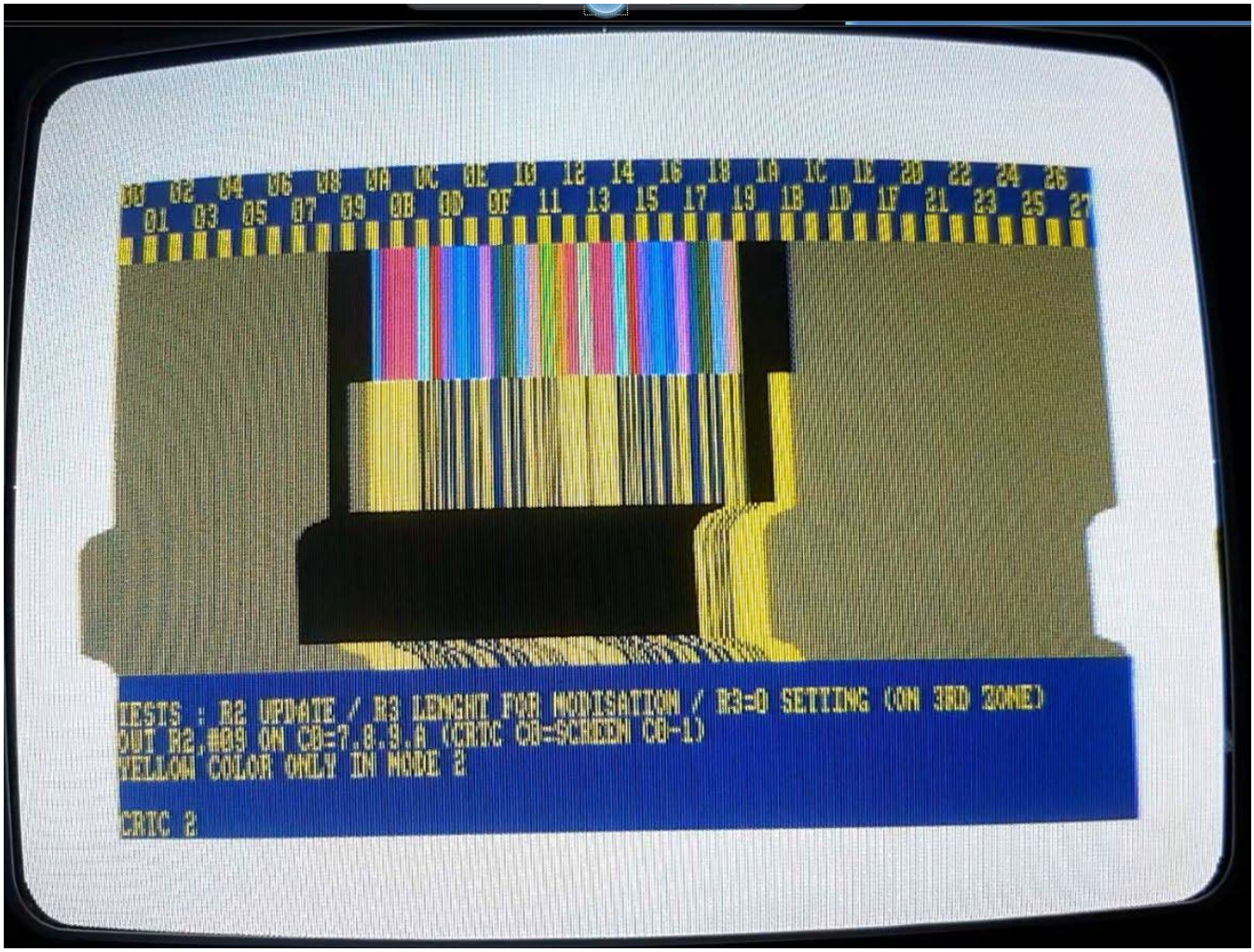
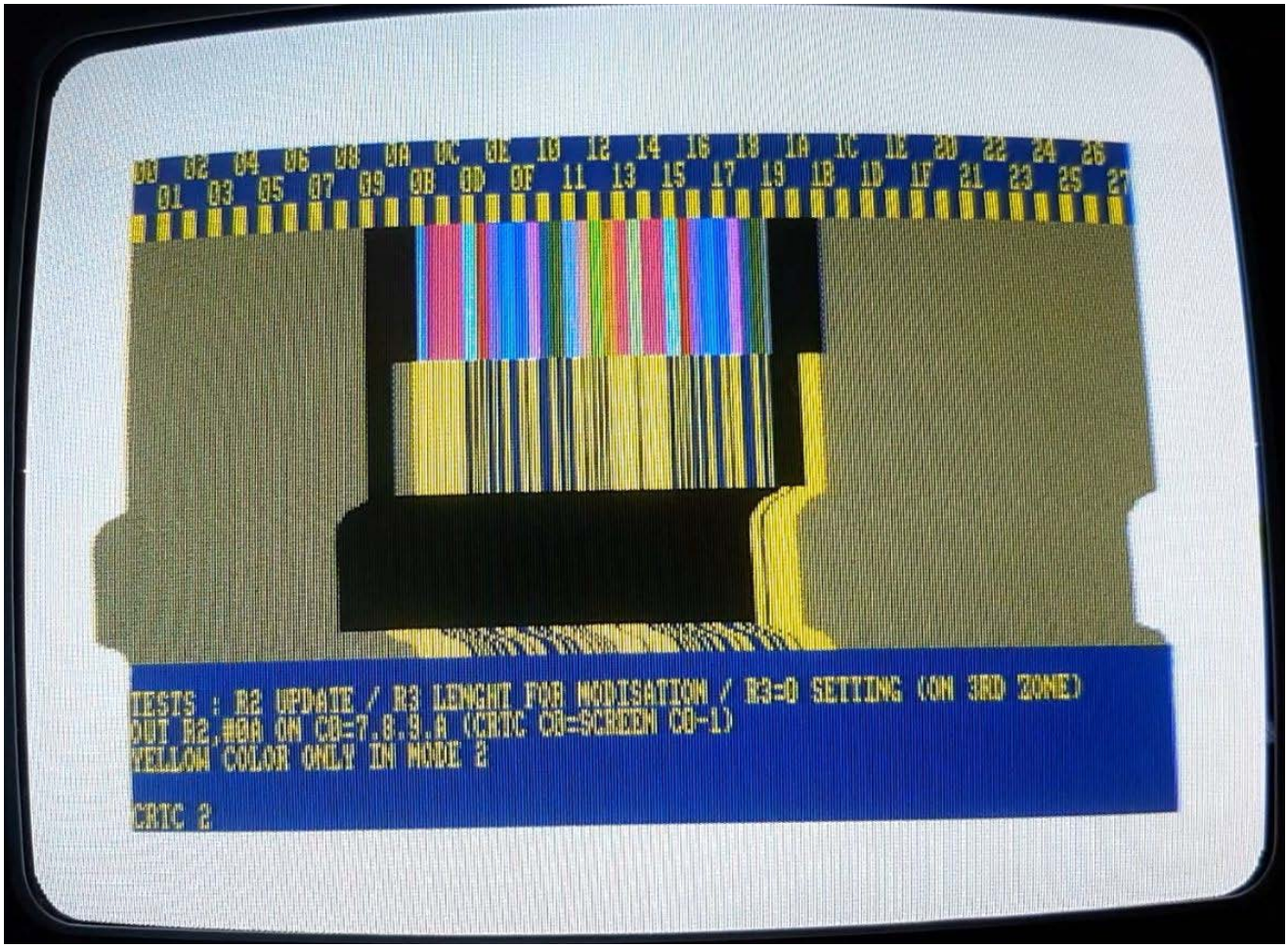
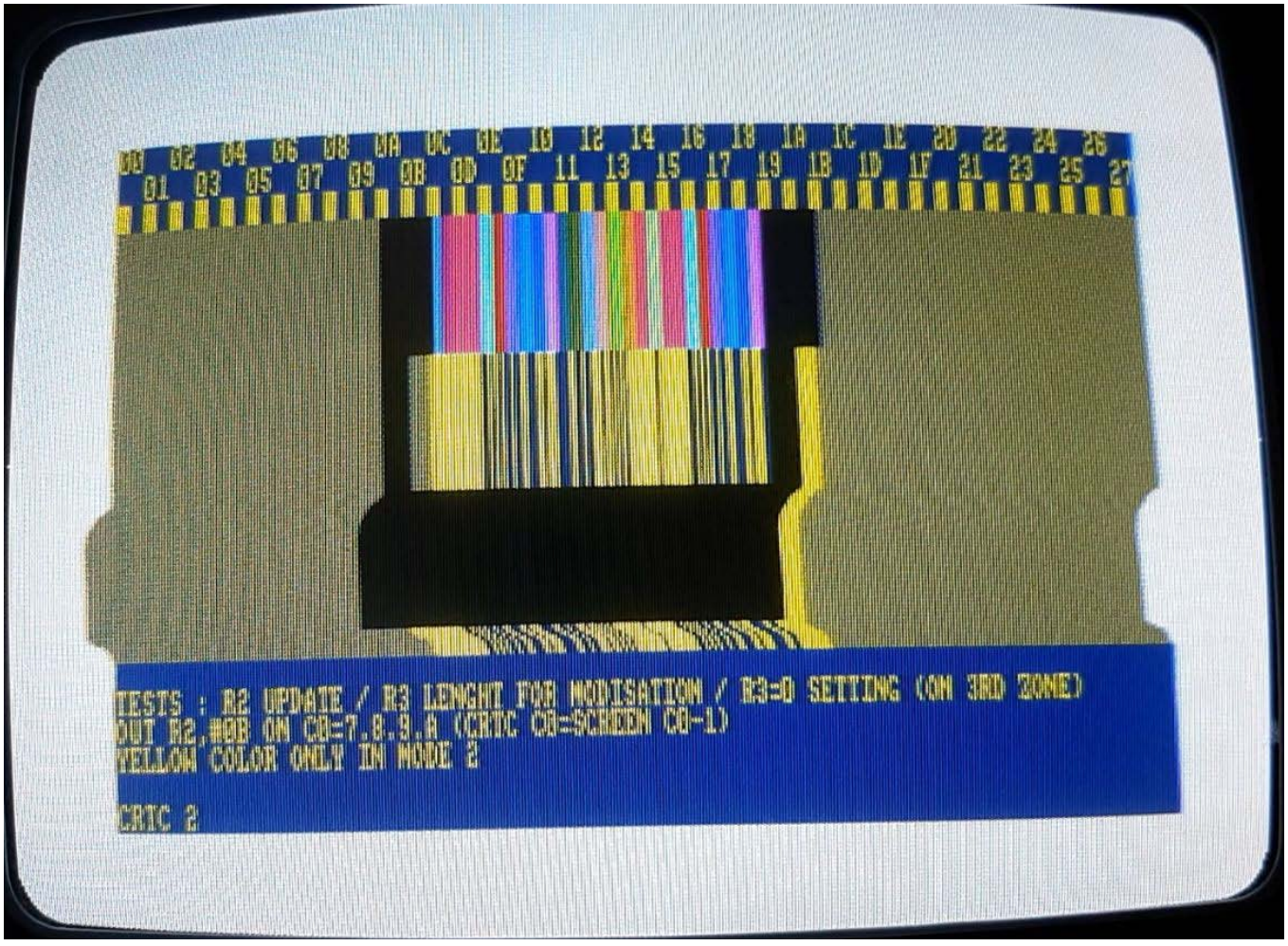
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

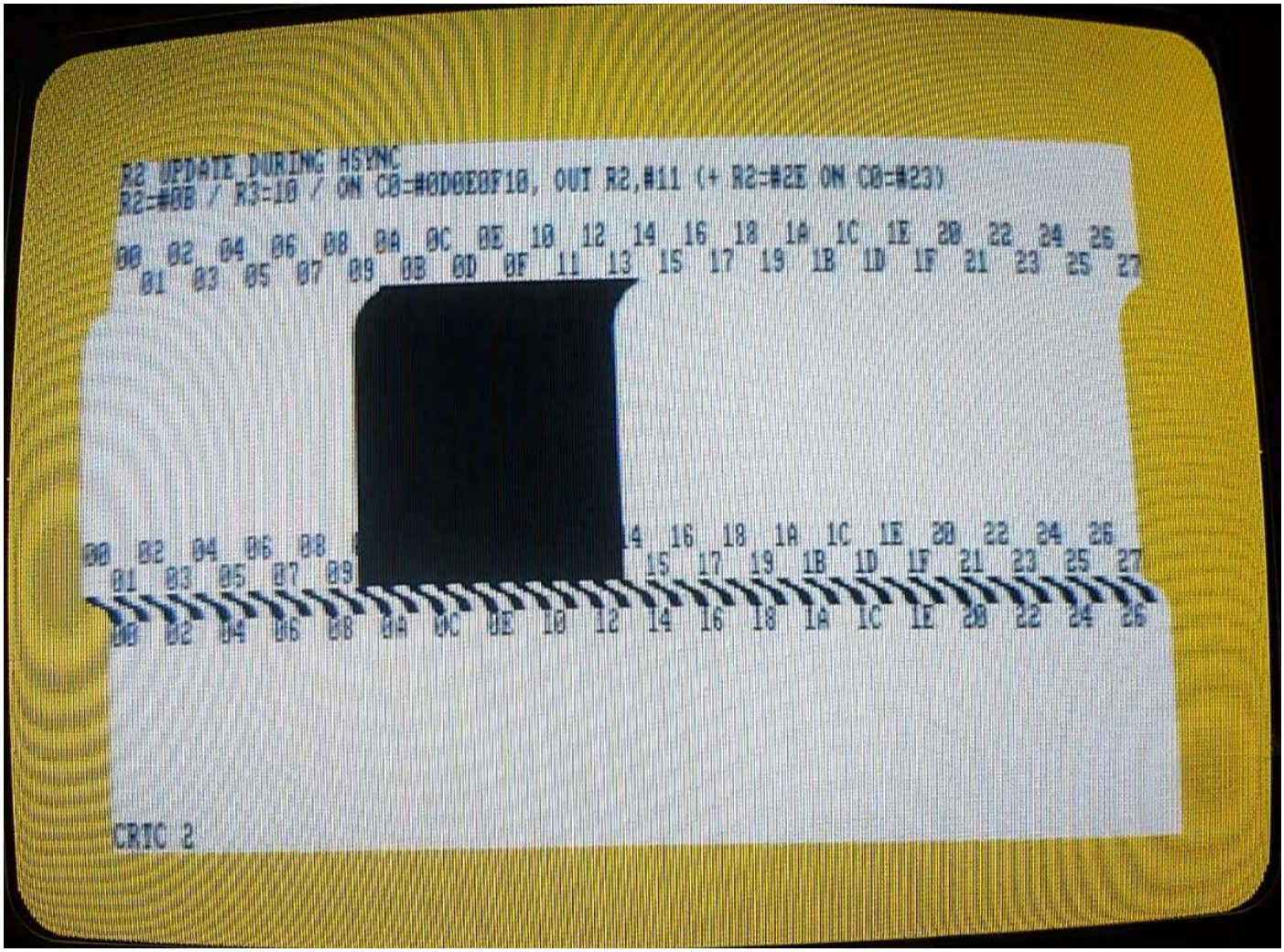


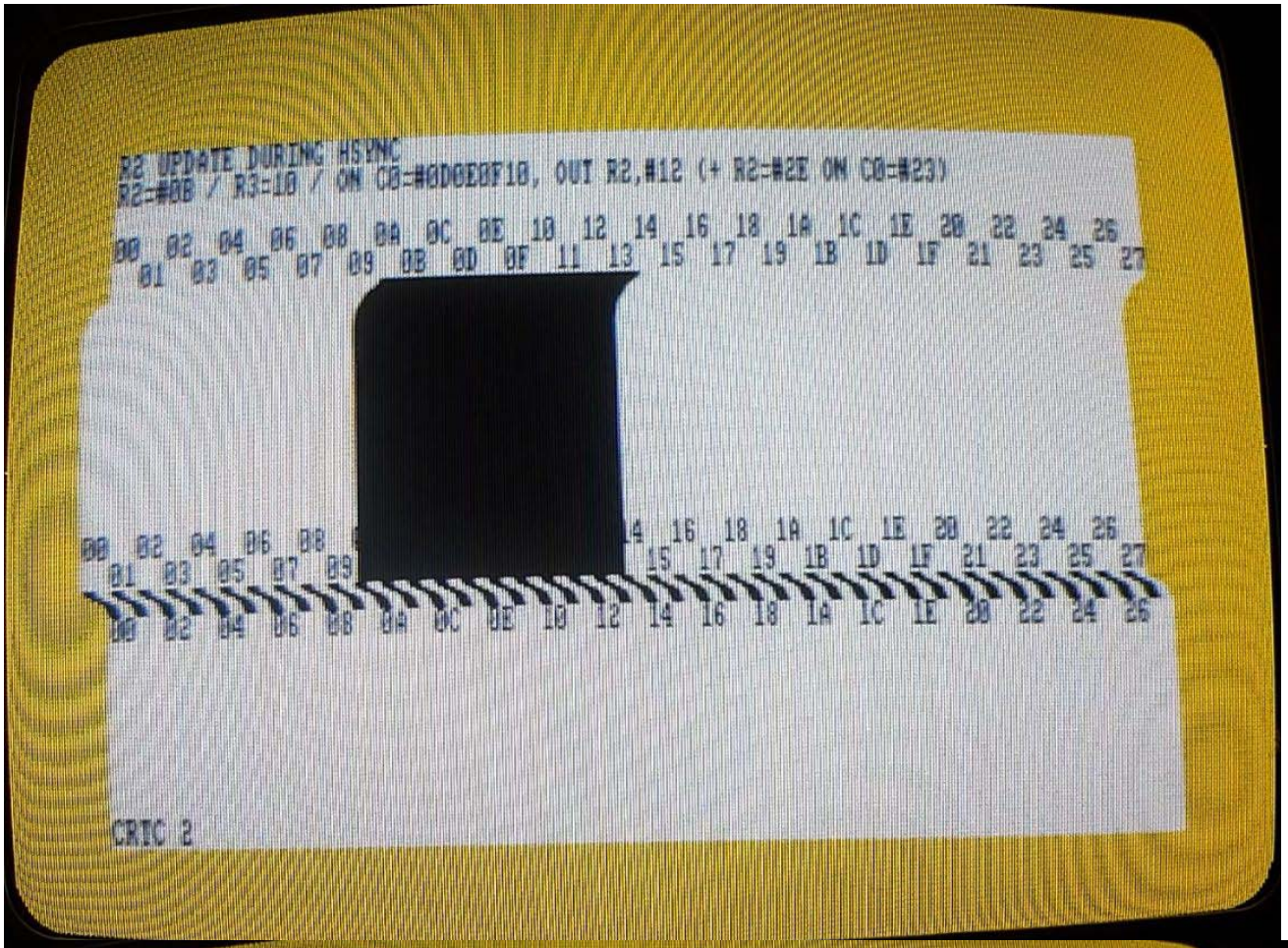

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
TESTS : R2 UPDATE / R3 LENGHT FOR MODISATION / R3=0 SETTING (ON 3RD ZONE)
OUT R2,#0A ON CR=7,8,9,A (CRTC C0=SCREEN C0-1)
YELLOW COLOR ONLY IN MODE 2
CRTC 2

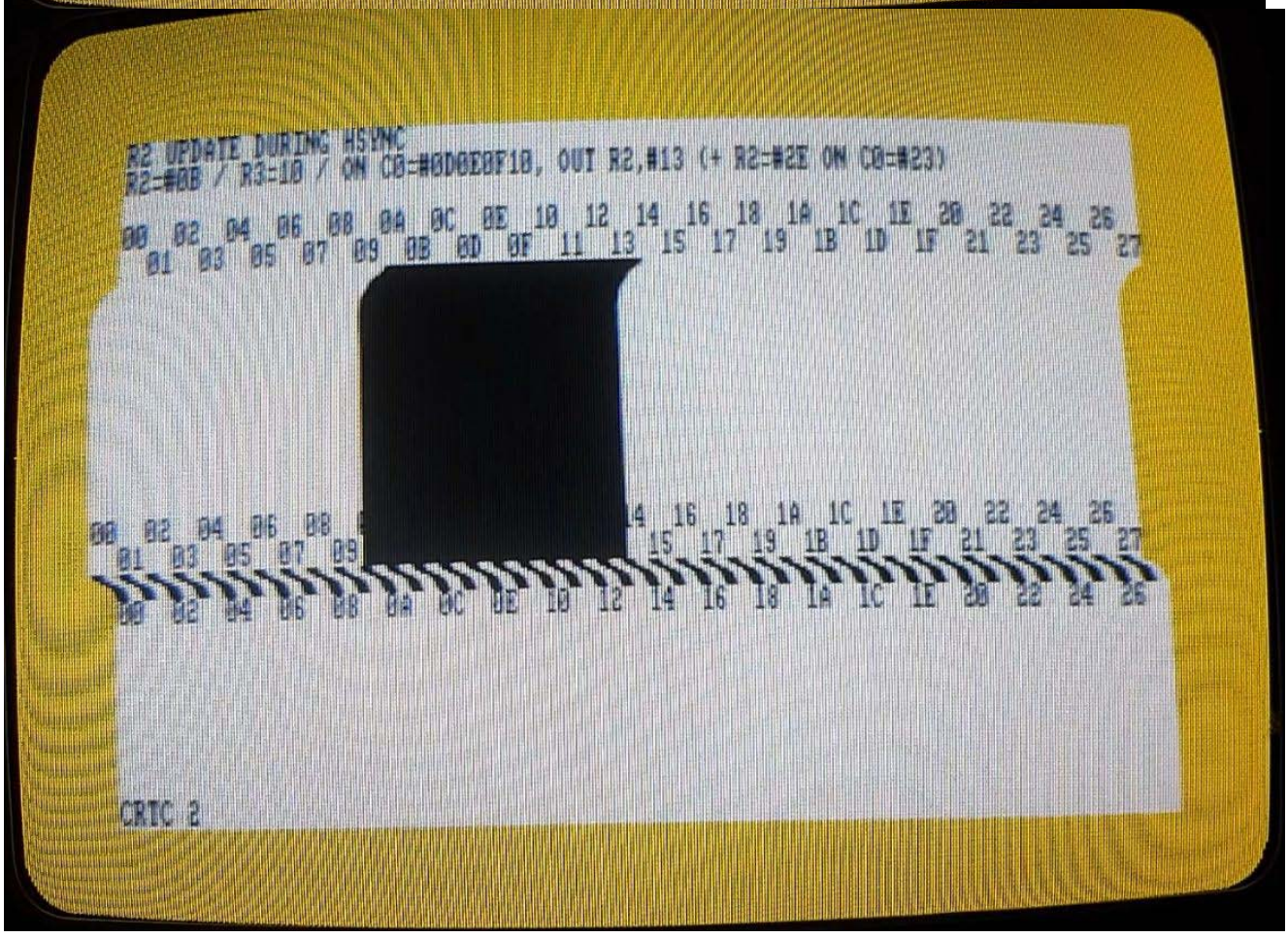

00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
TESTS : R2 UPDATE / R3 LENGHT FOR MODISATION / R3=0 SETTING (ON 3RD ZONE)
OUT R2,#0B ON CR=7,8,9,A (CRTC C0=SCREEN C0-1)
YELLOW COLOR ONLY IN MODE 2
CRTC 2

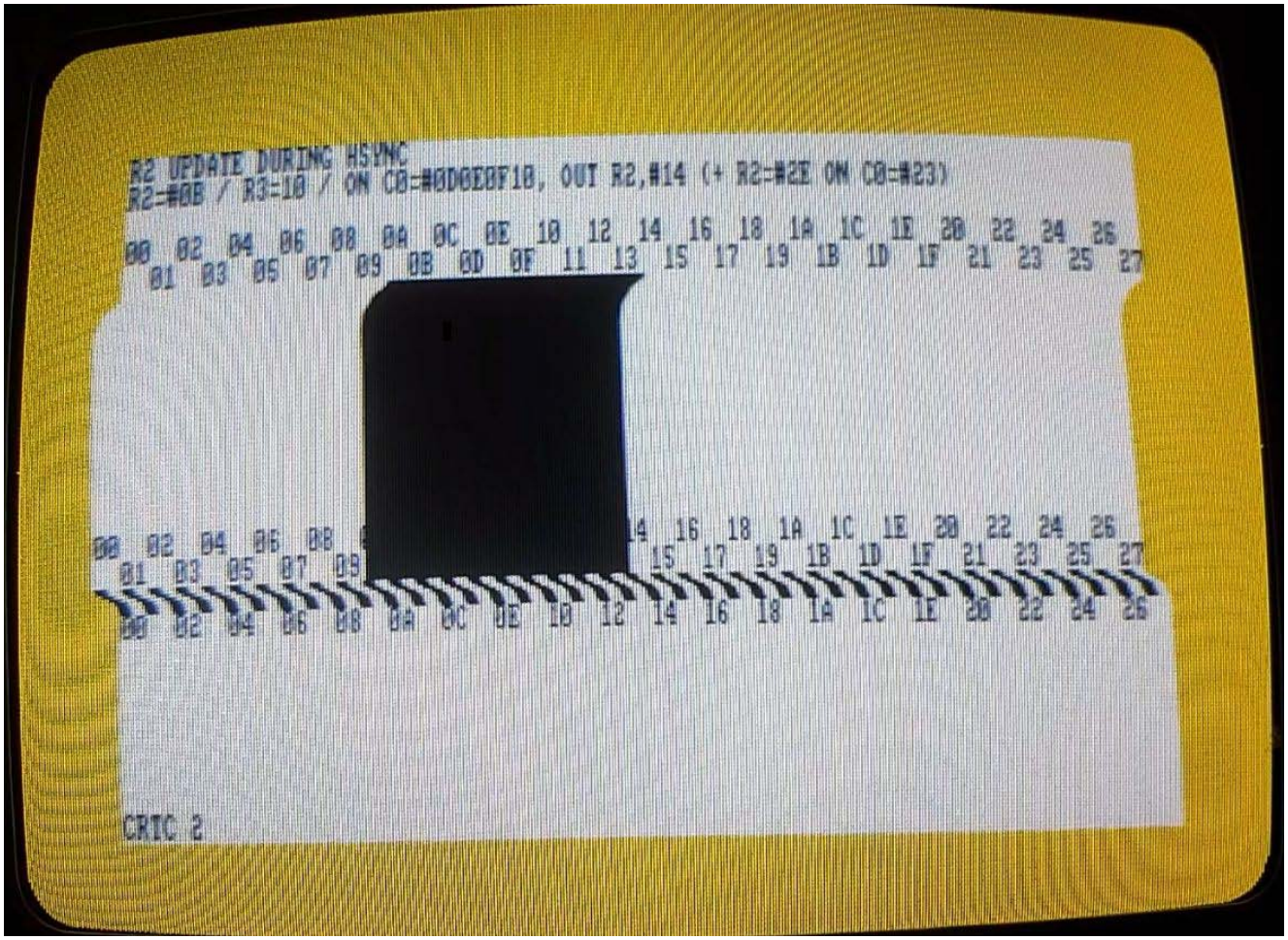
R2 UPDATE DURING & AFTER HSYNC

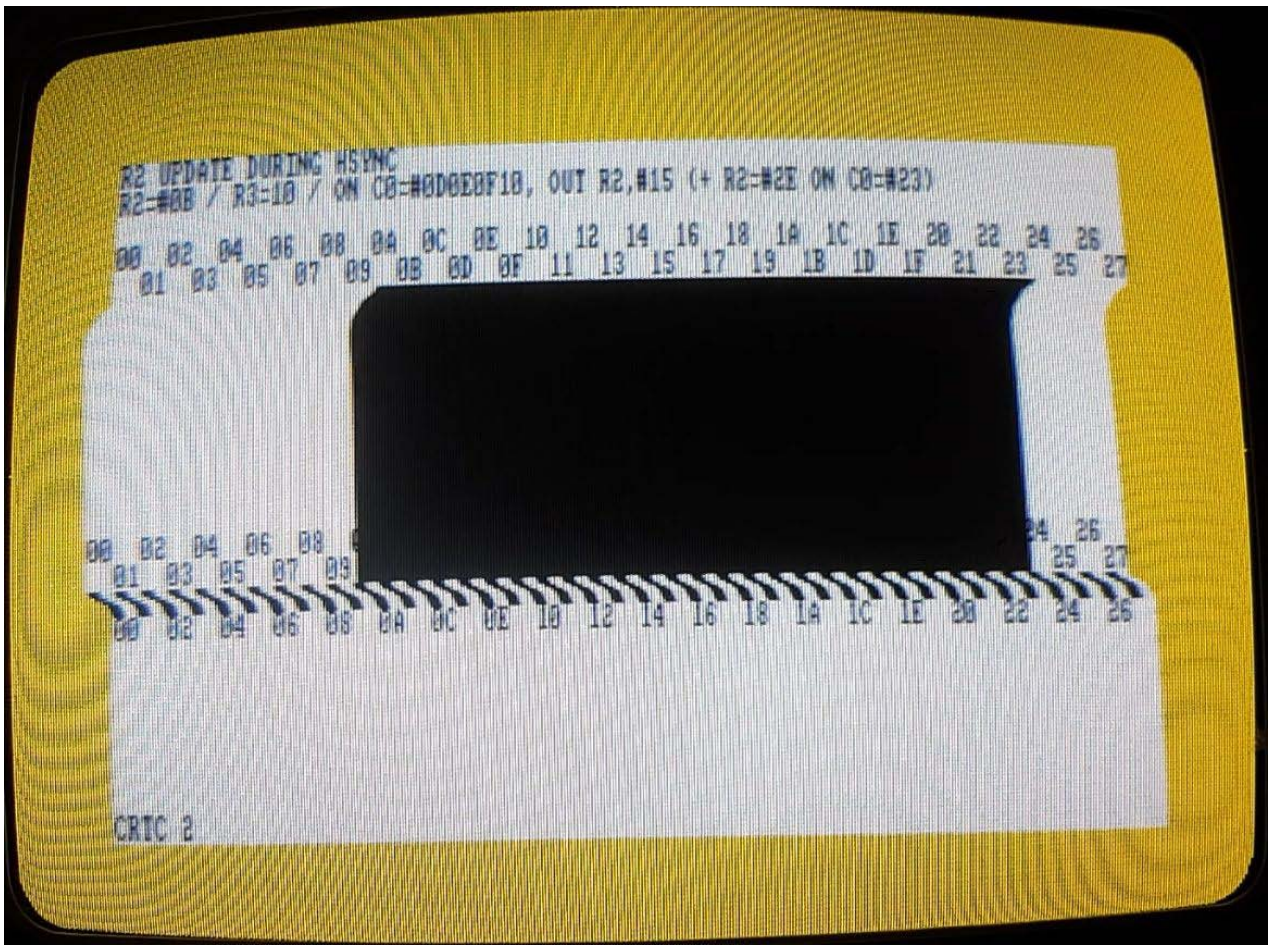
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

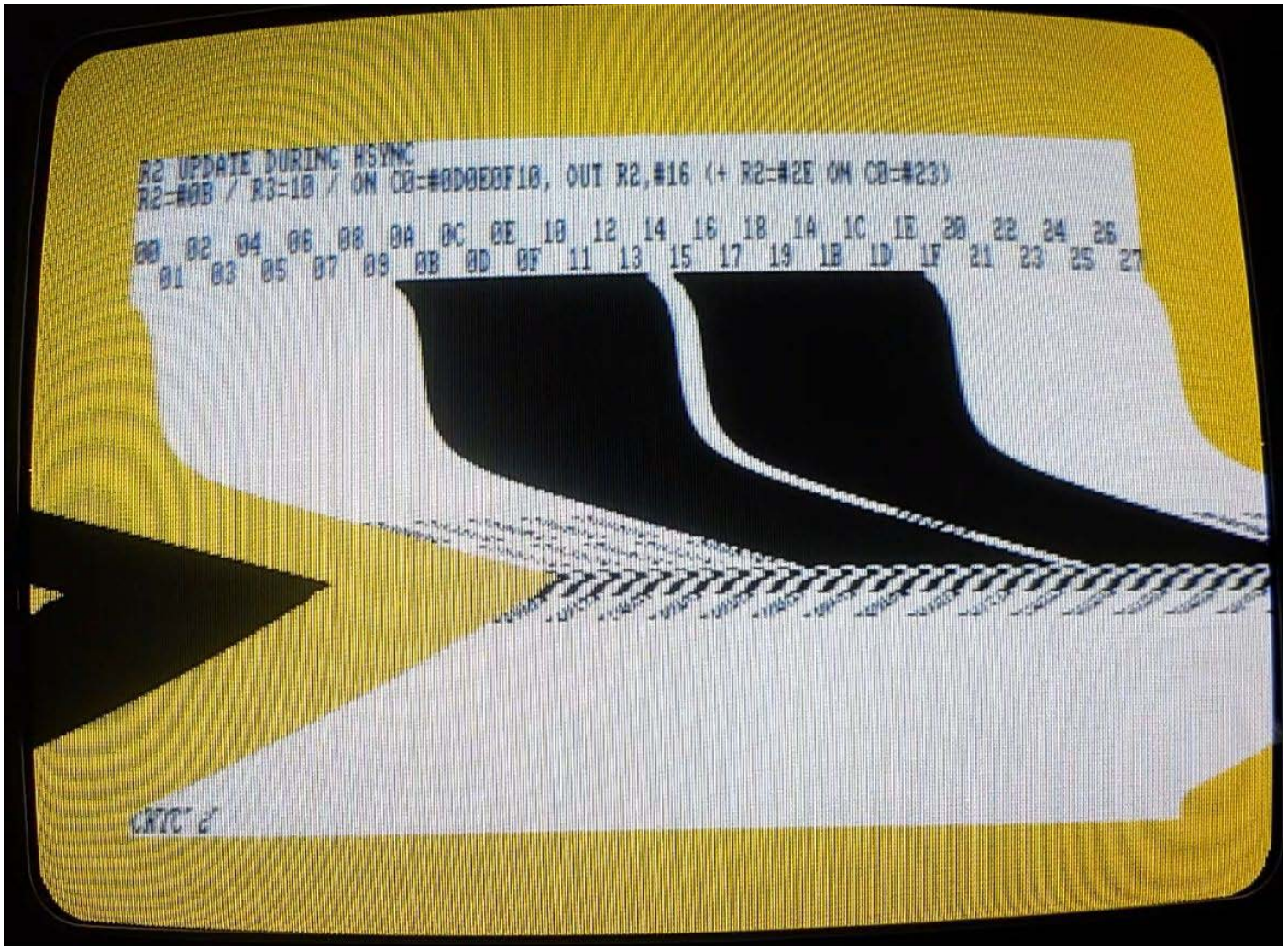



R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#12 (+ R2=#2E ON C0=#23)
CRTC 2


R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#13 (+ R2=#2E ON C0=#23)
CRTC 2

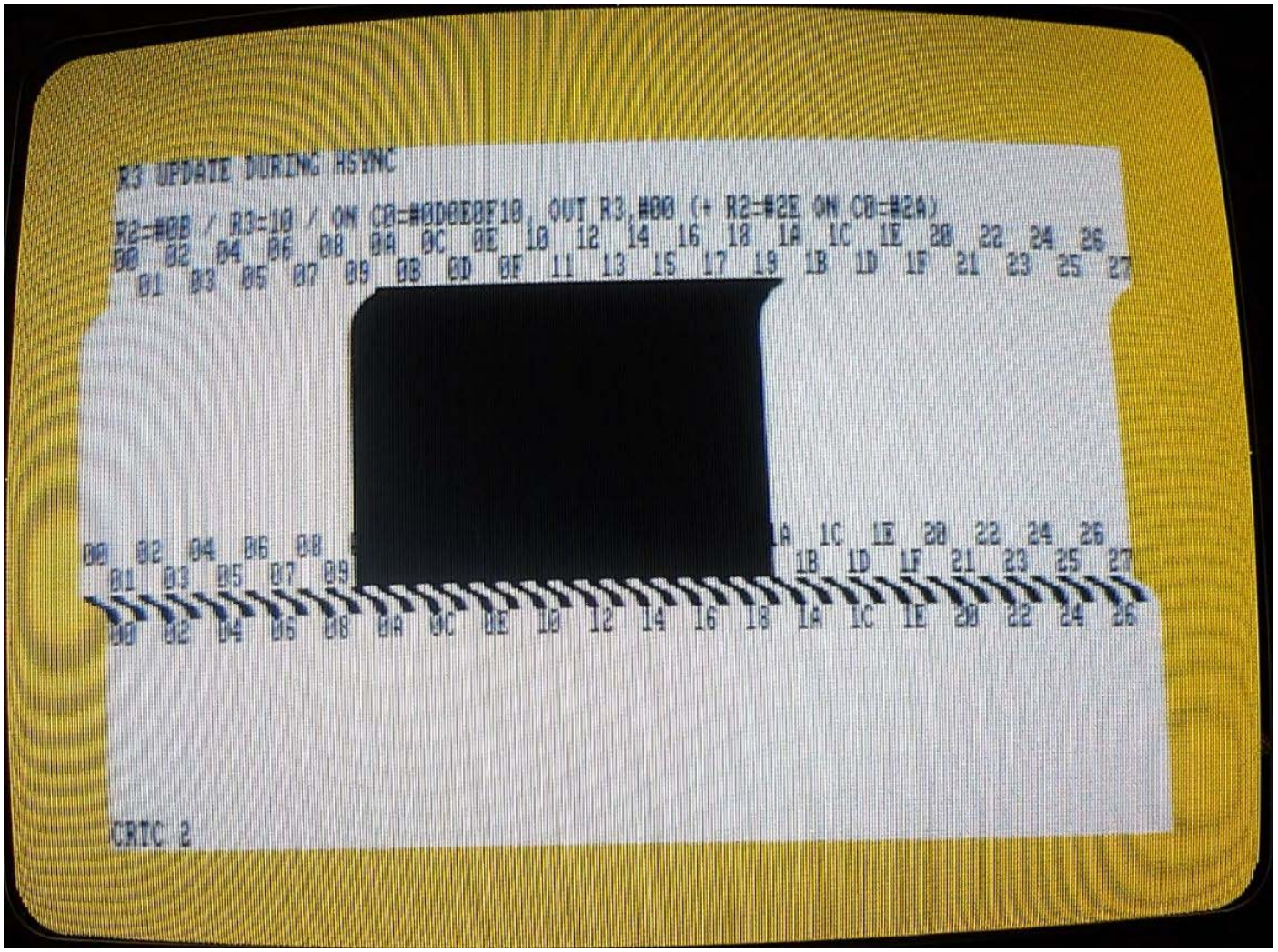

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#14 (+ R2=#2E ON C0=#23)
CRTC 2

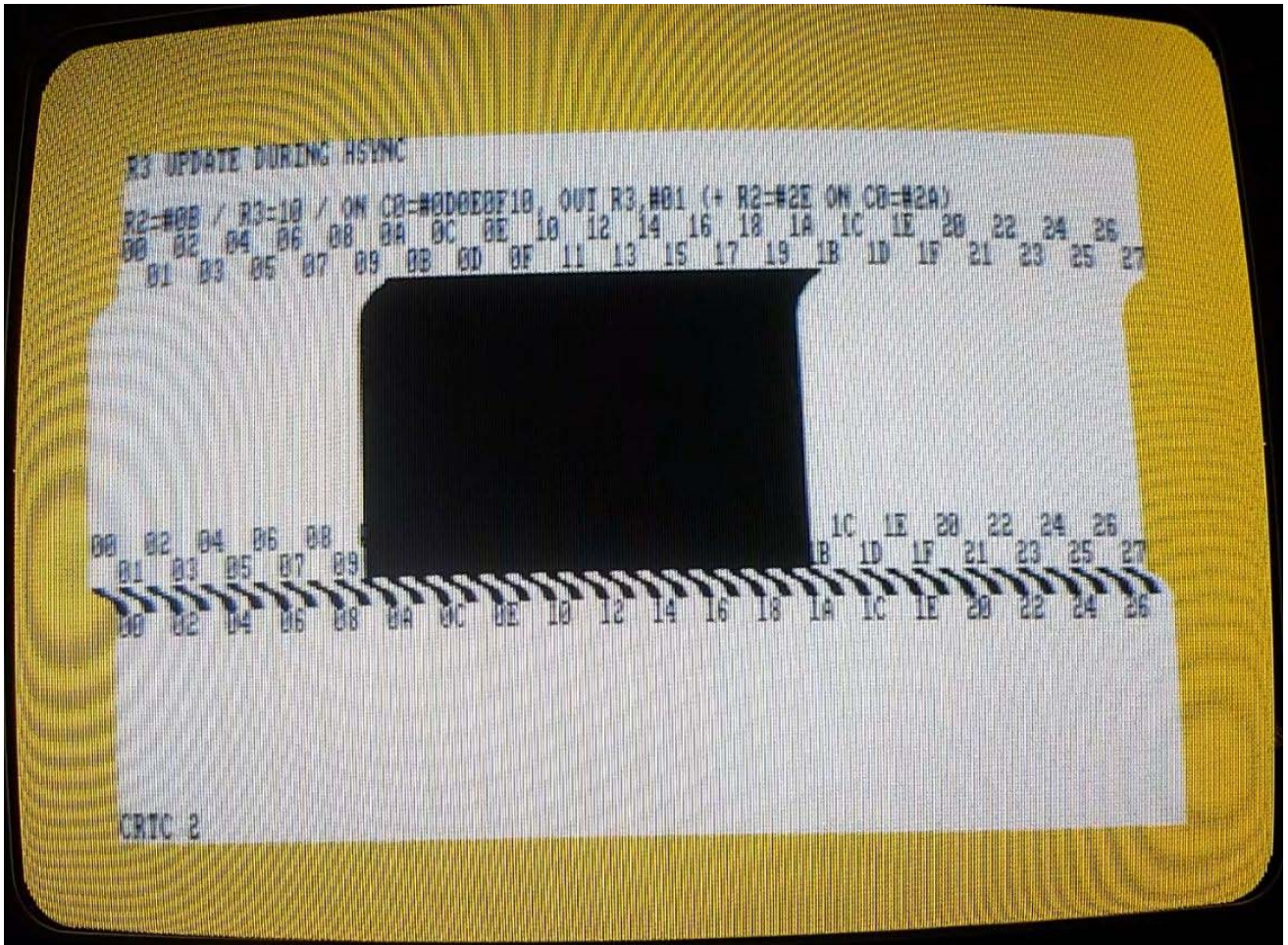

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#15 (+ R2=#2E ON C0=#23)
CRTC 2

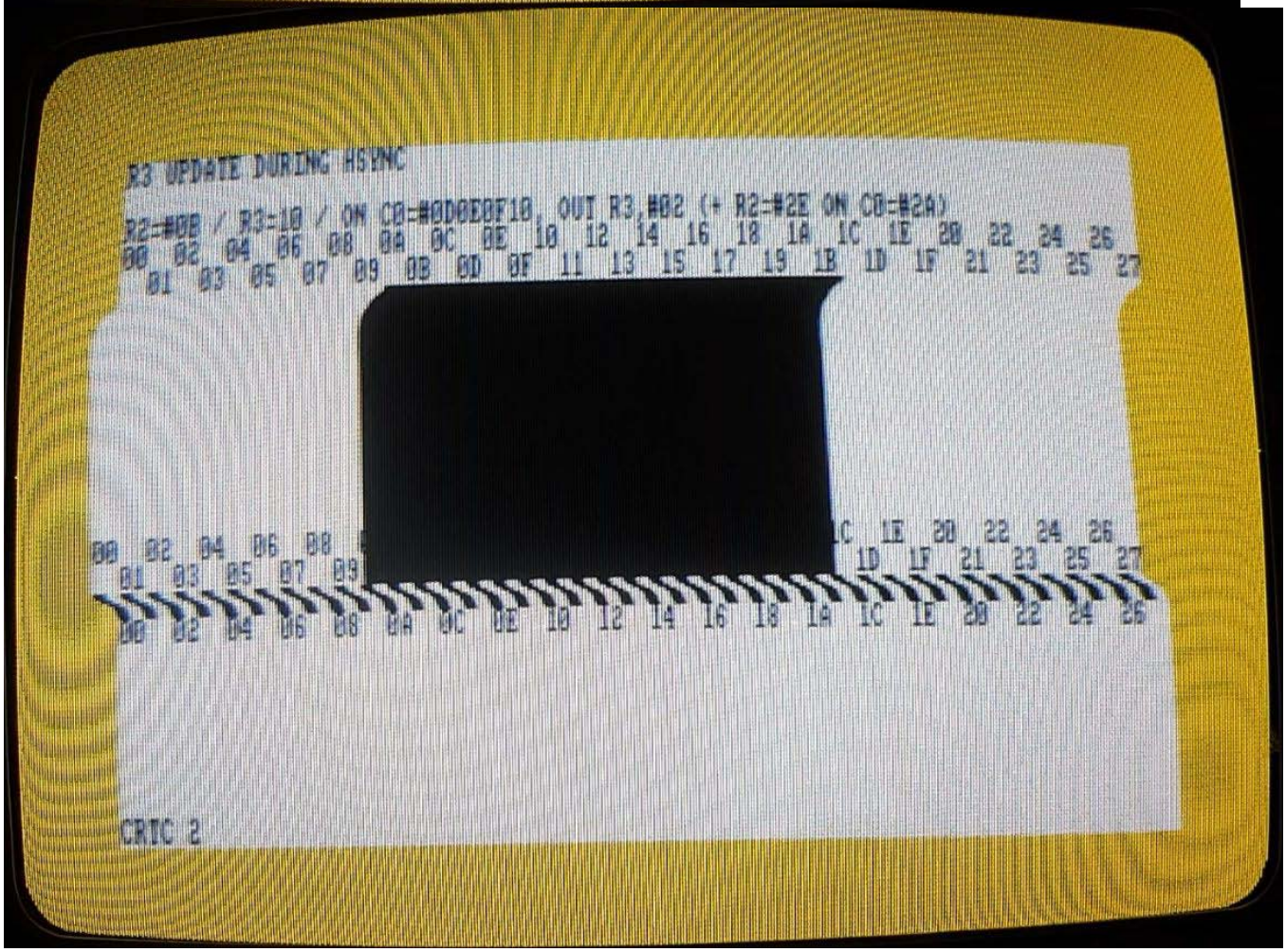

R2 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R2,#16 (+ R2=#2E ON C0=#23)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 2

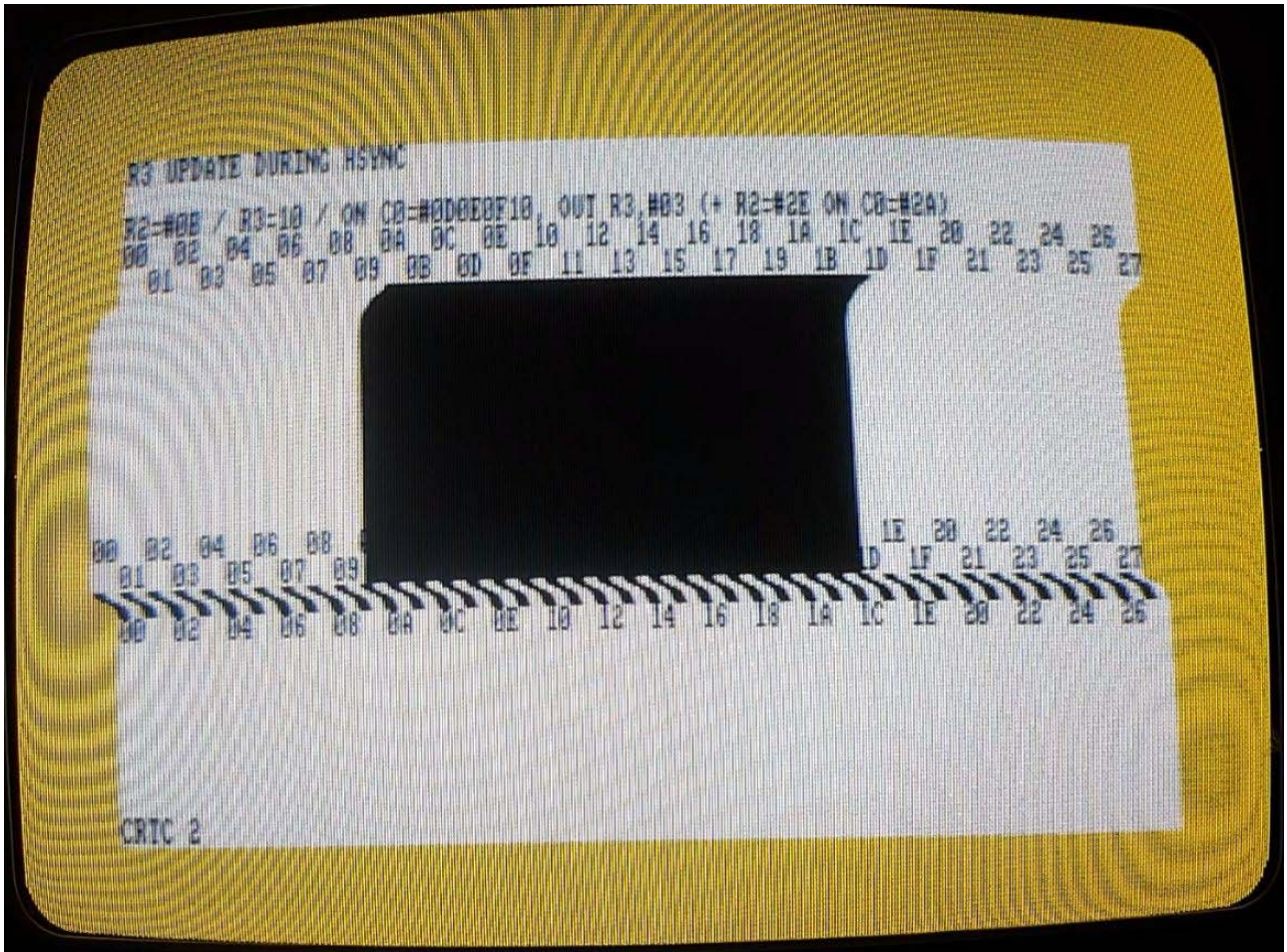
R3 UPDATE DURING HSYNC

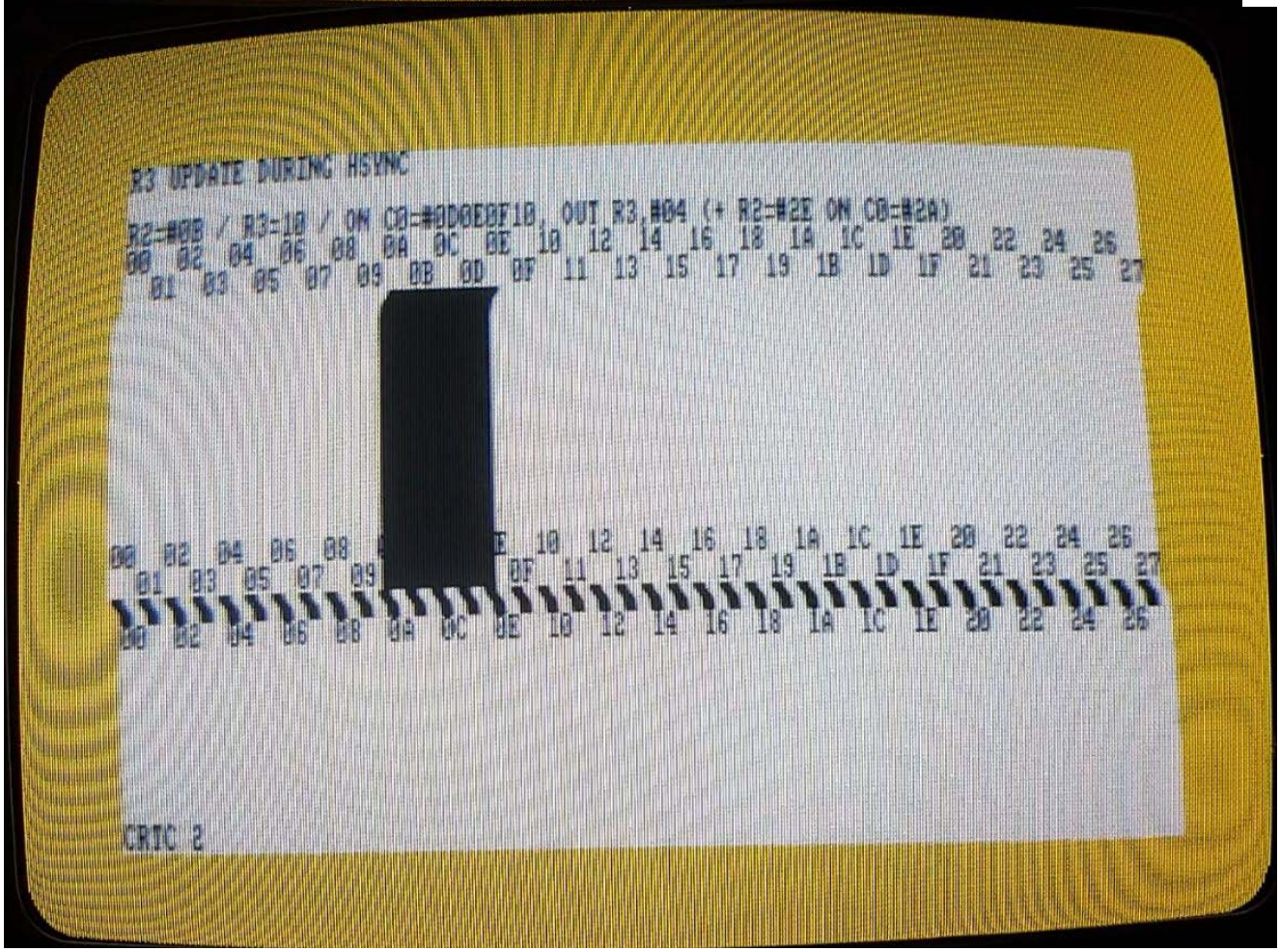
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

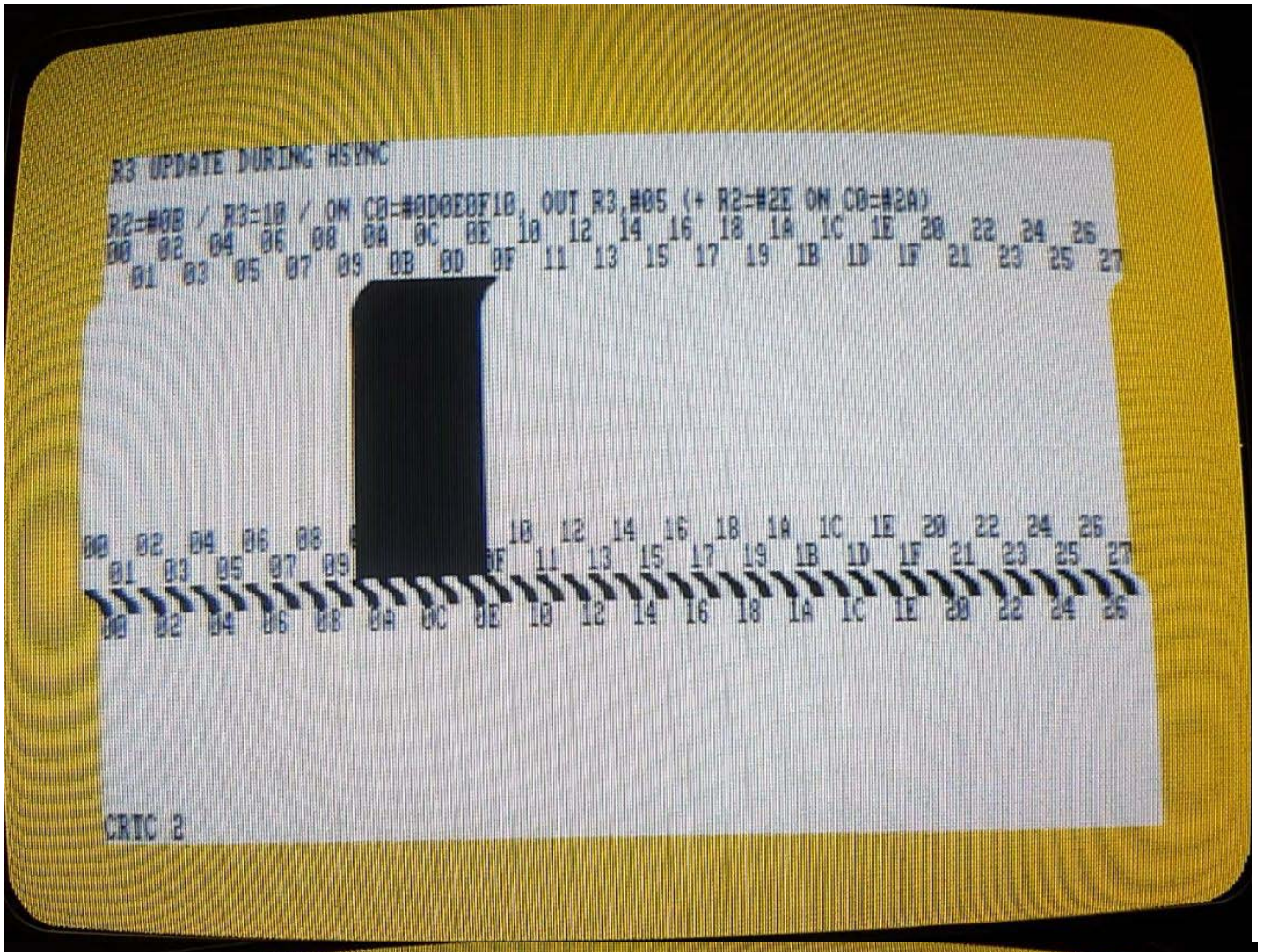


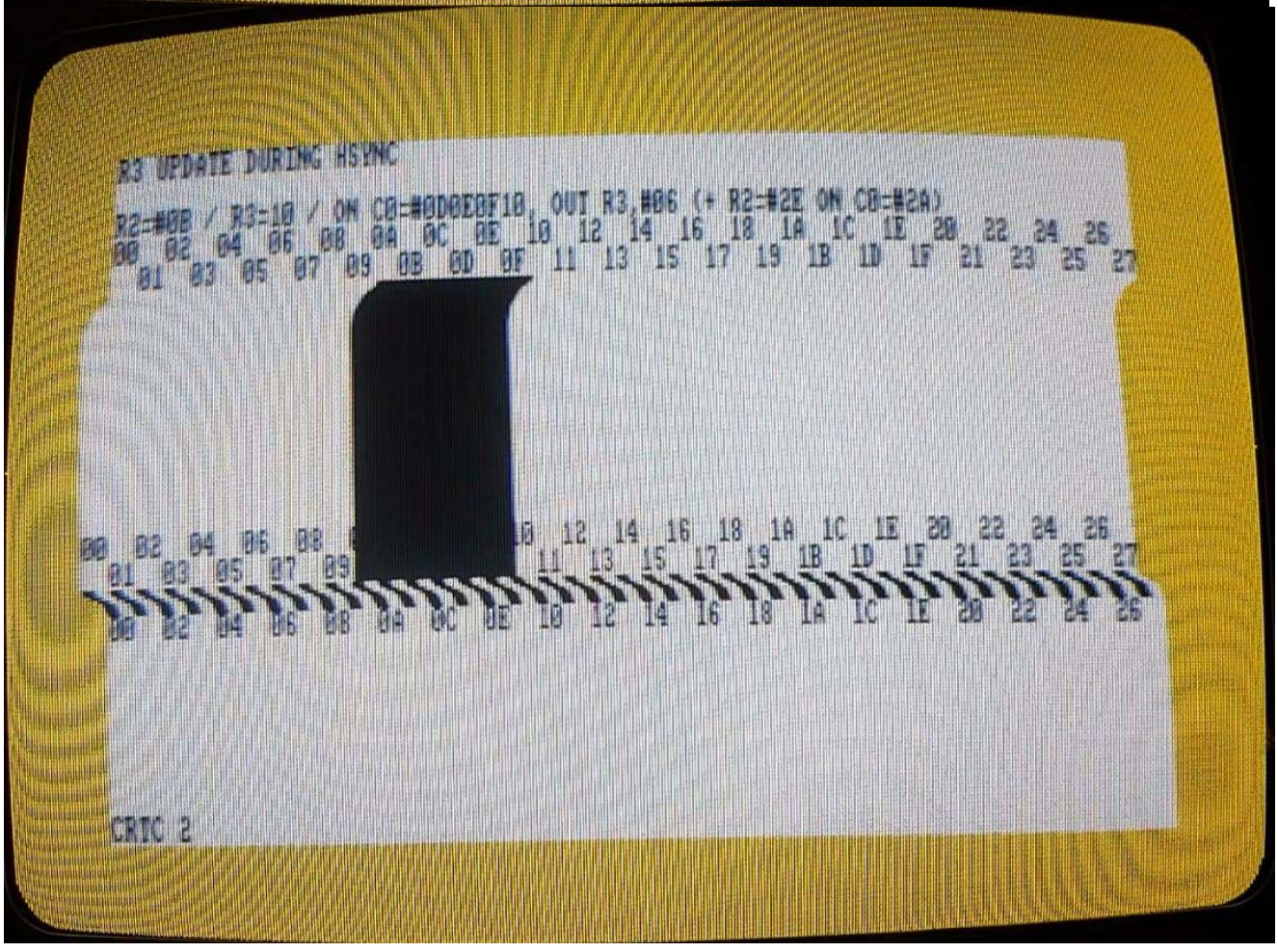

R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#01 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
CRTC 2

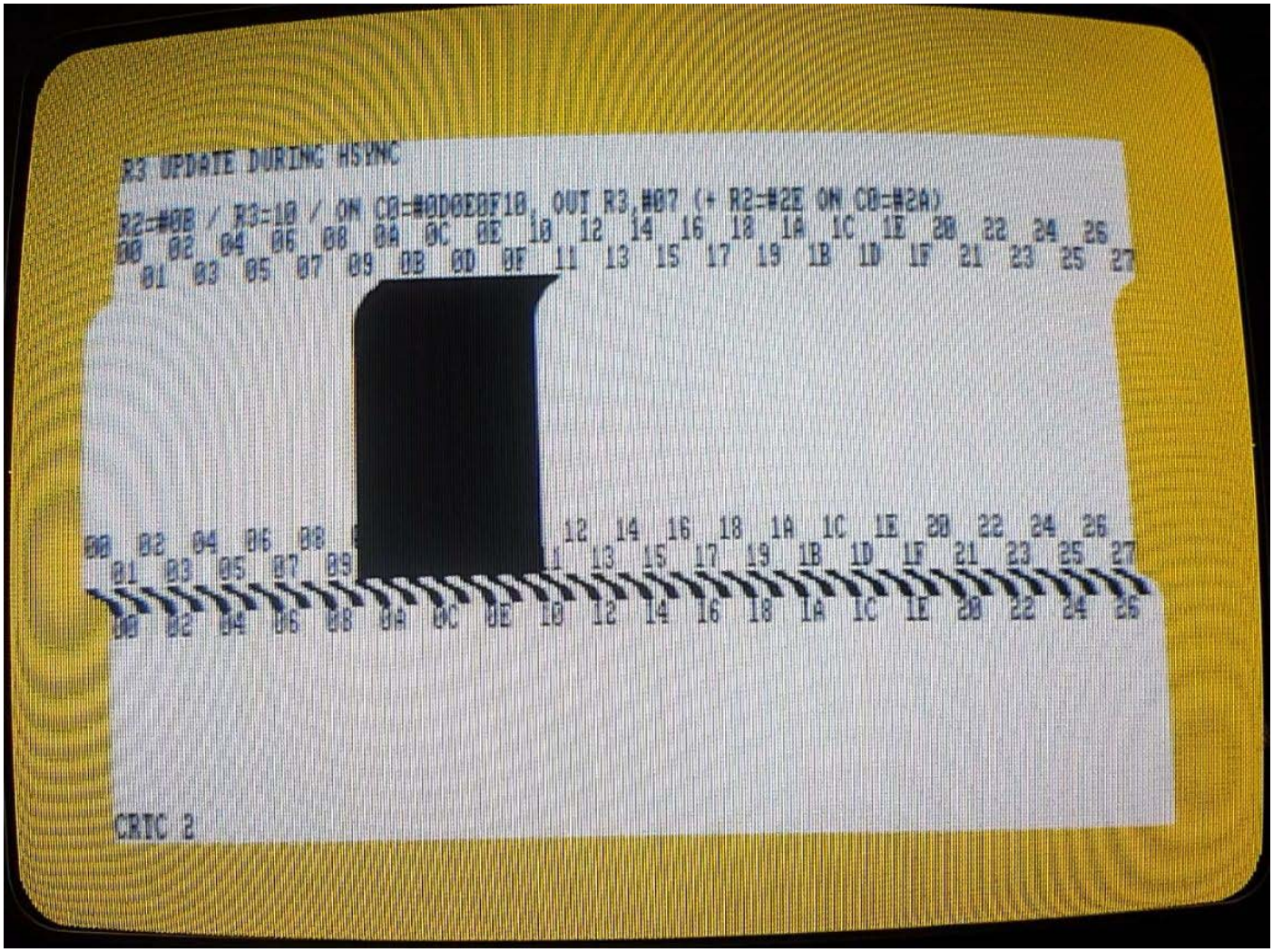

R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#02 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
CRTC 2


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#03 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 2


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#04 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 2

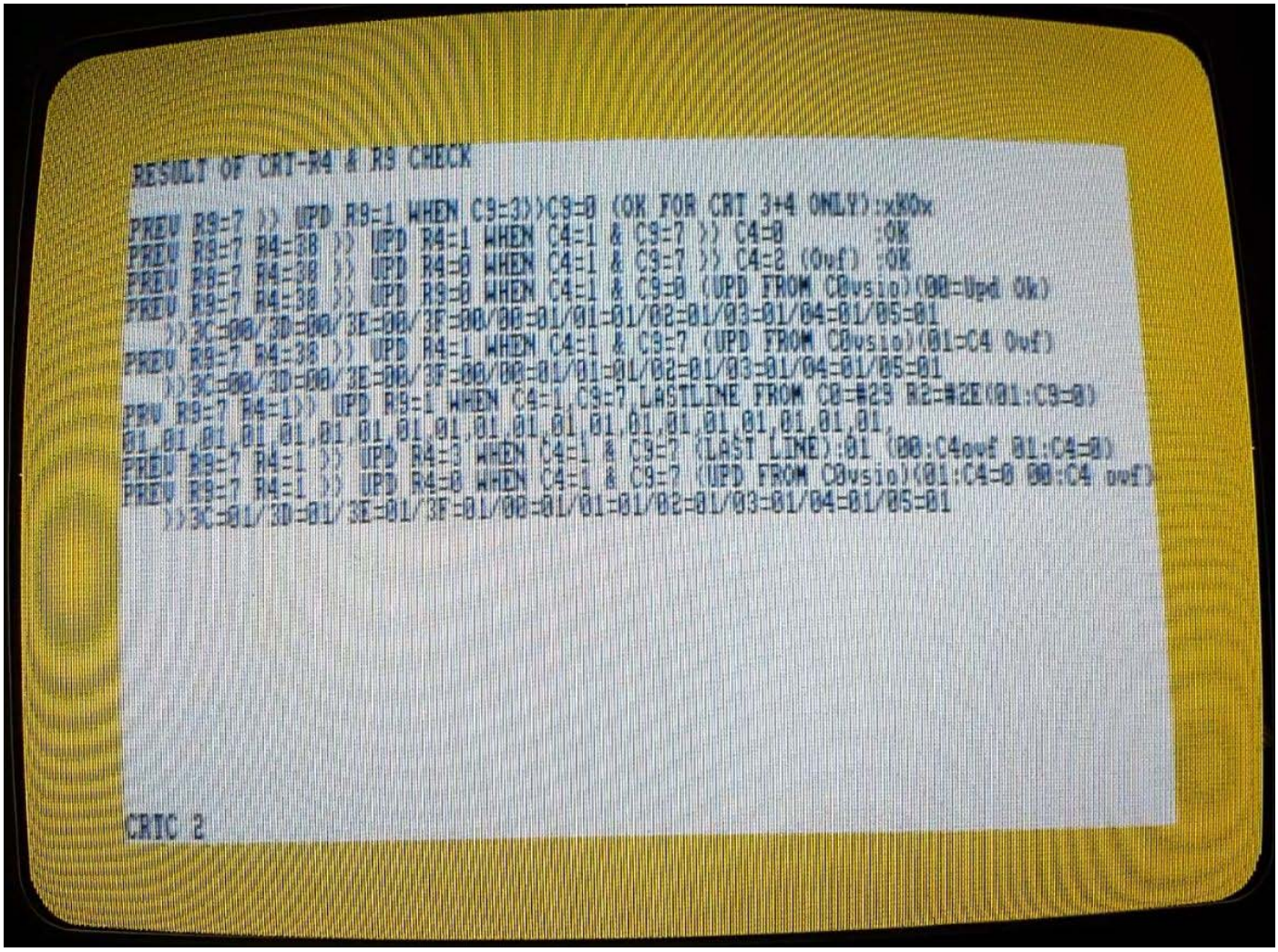

R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R3,#05 (+ R2=#2E ON CB=#2A)
CRTC 2


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON CB=#0D0E0F10, OUT R3,#06 (+ R2=#2E ON CB=#2A)
CRTC 2


R3 UPDATE DURING HSYNC
R2=#0B / R3=10 / ON C0=#0D0E0F10, OUT R3,#07 (+ R2=#2E ON C0=#2A)
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
CRTC 2

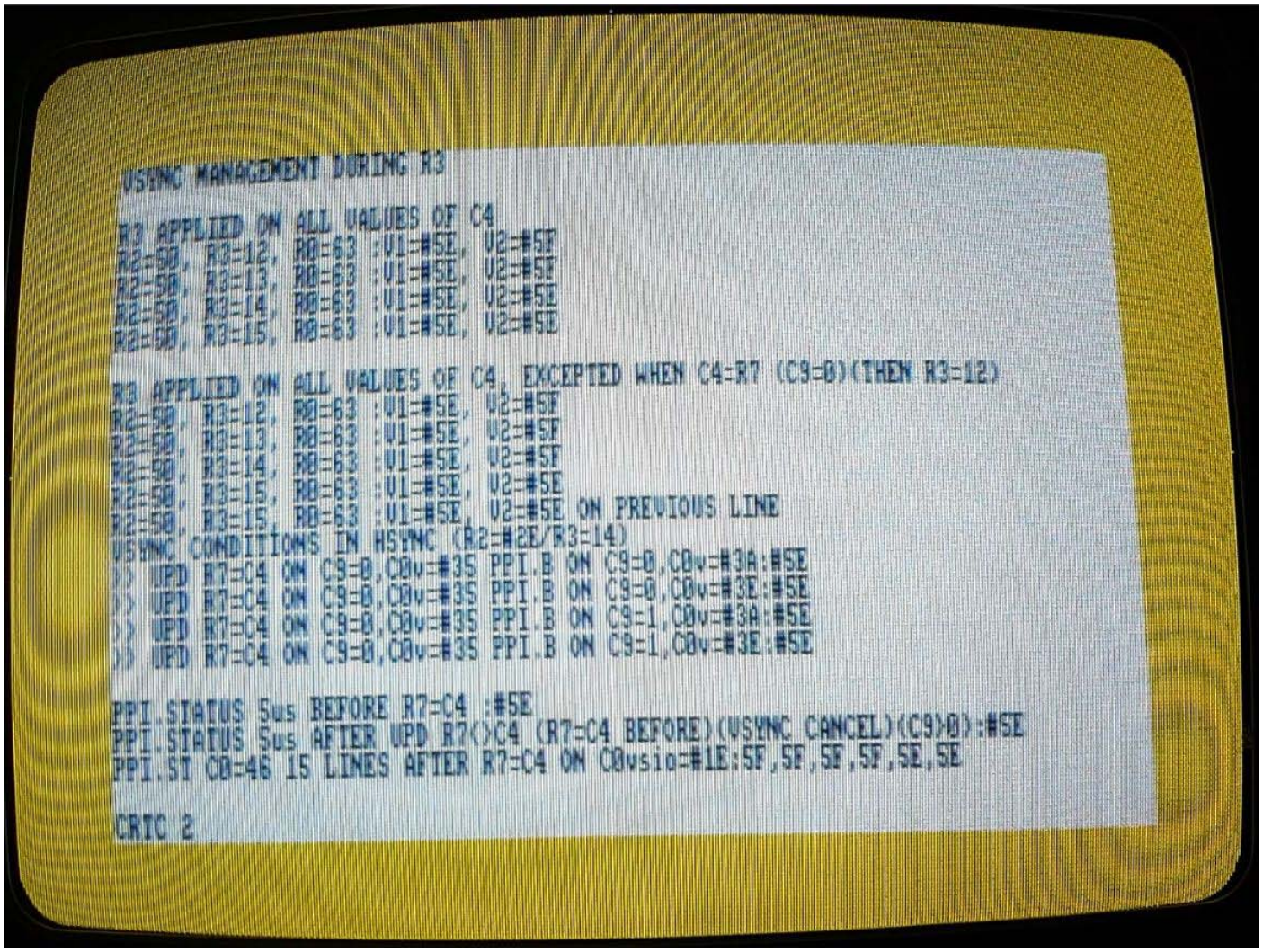
R4 & R9 CHECKING

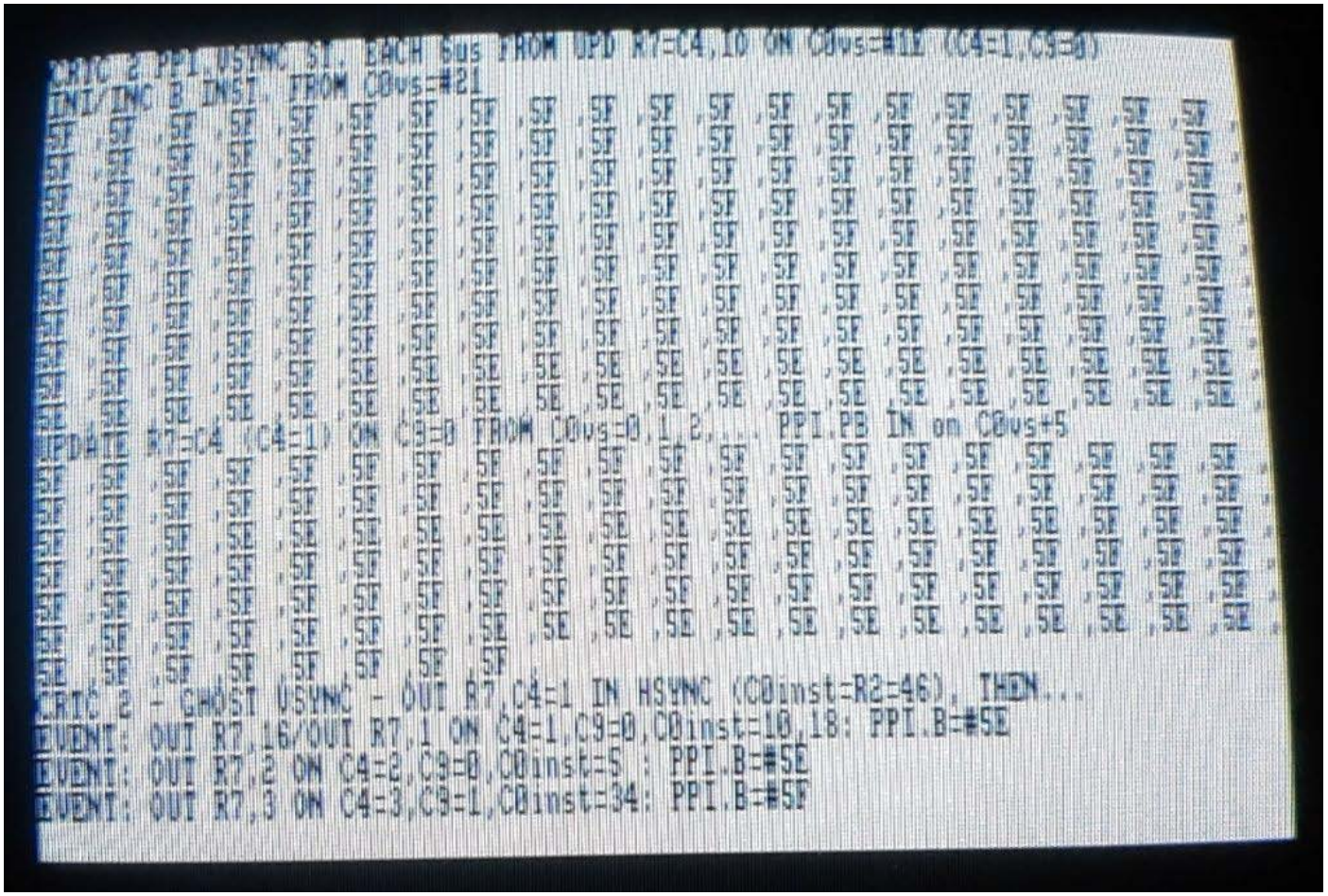
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



VSYNC CONDITIONS

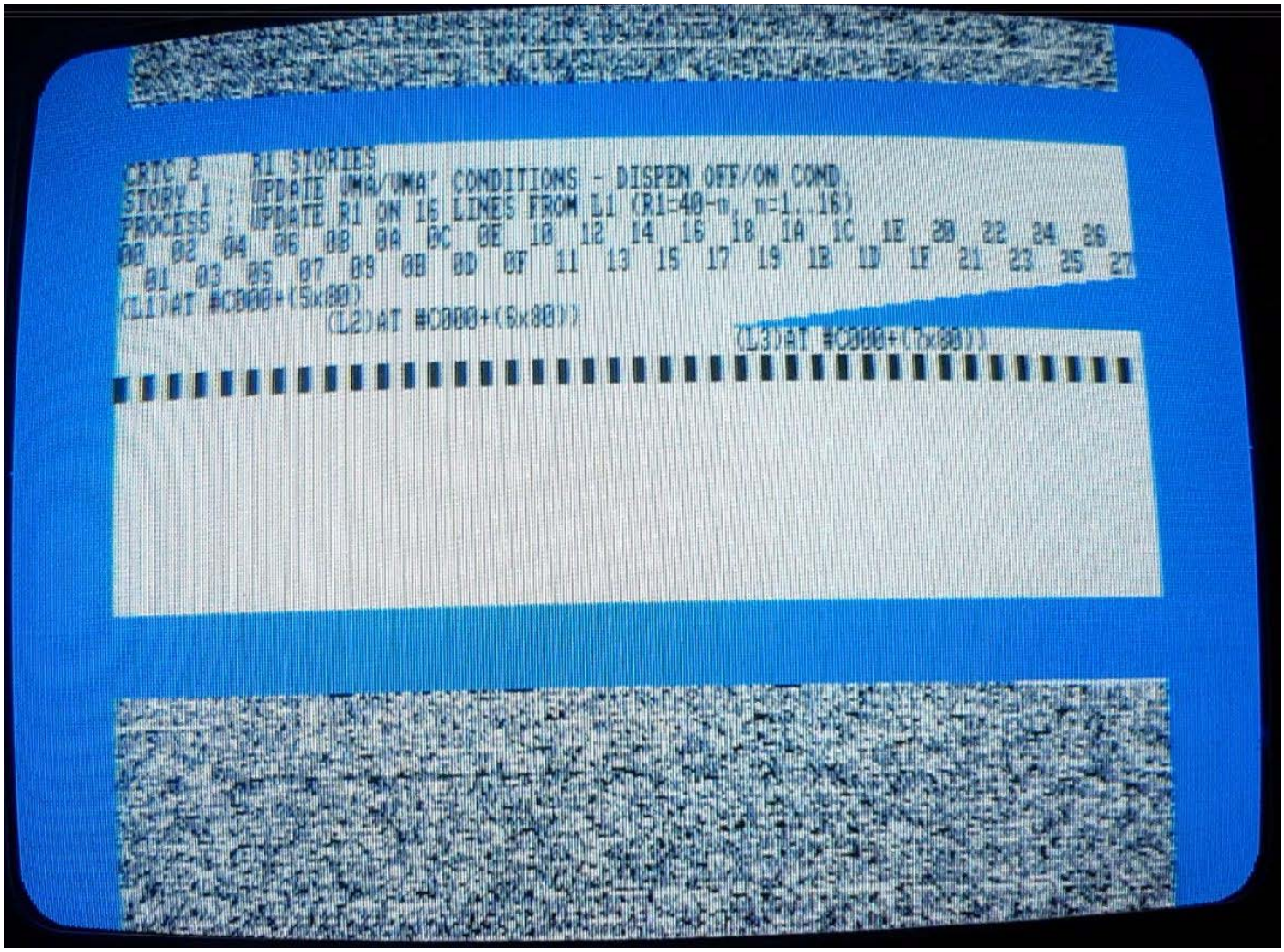
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

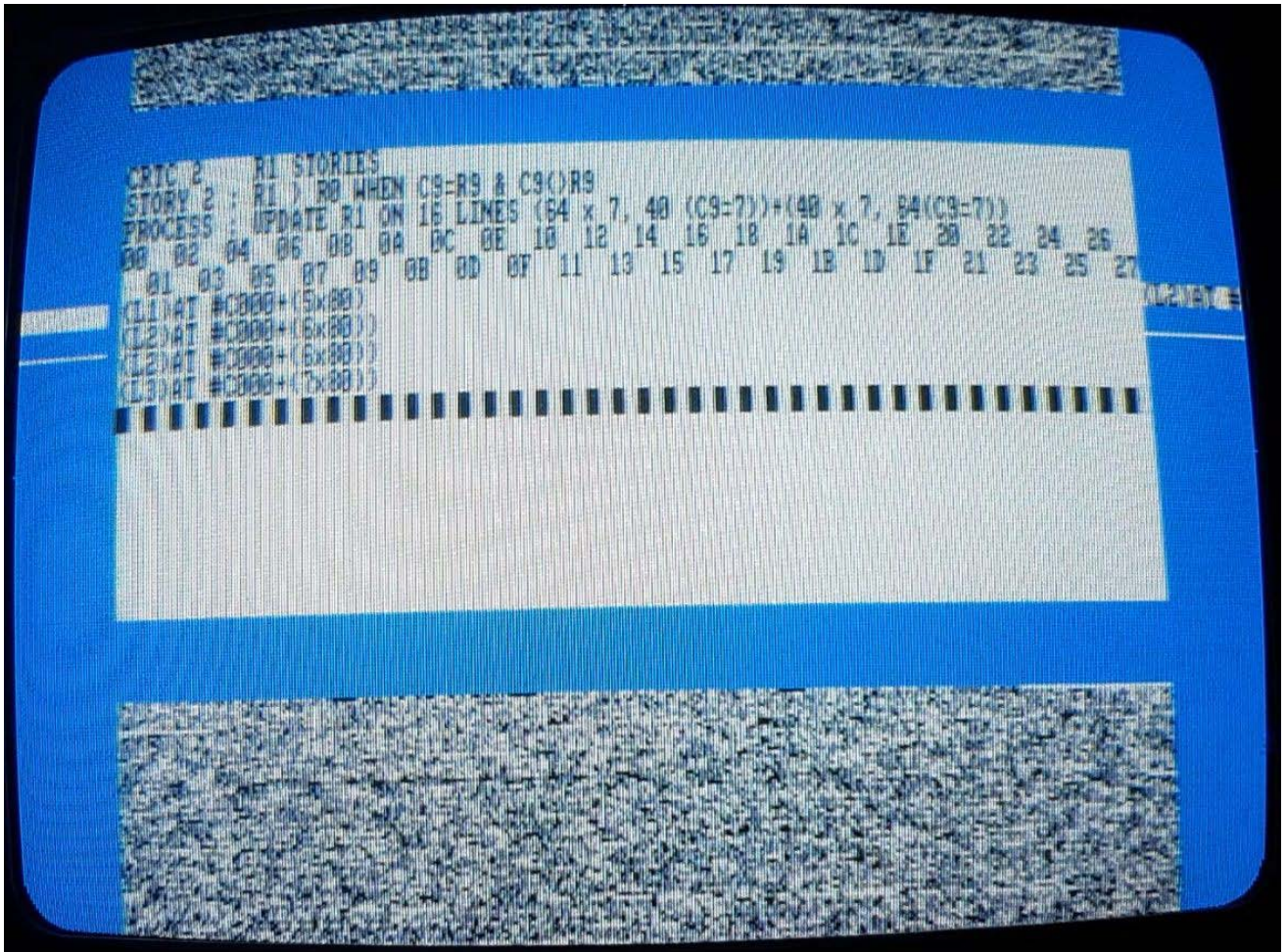



CRTC 2 PPI.VSYNC SI. EACH 6us FROM DPO RY=C4,10 ON C0vs=#12 (C4=1,C6=0)
INIT/INC 8 INST. FROM C0vs=#21
DPO R7=C4 (C4=1) OR (C4=0 FROM C0vs=0,1,2,... PPI.PB IN on C0vs+5
CRTC 2 - GHOST VSYNC - OUT R7,C4=1 IN HSYNC (C0inst=R2=46), THEN...
EVENT: OUT R7,16/OUT R7,1 ON C4=1,C9=0,C0inst=10,18: PPI.B=#5E
EVENT: OUT R7,2 ON C4=2,C9=0,C0inst=5 : PPI.B=#5E
EVENT: OUT R7,3 ON C4=3,C9=1,C0inst=34: PPI.B=#5F

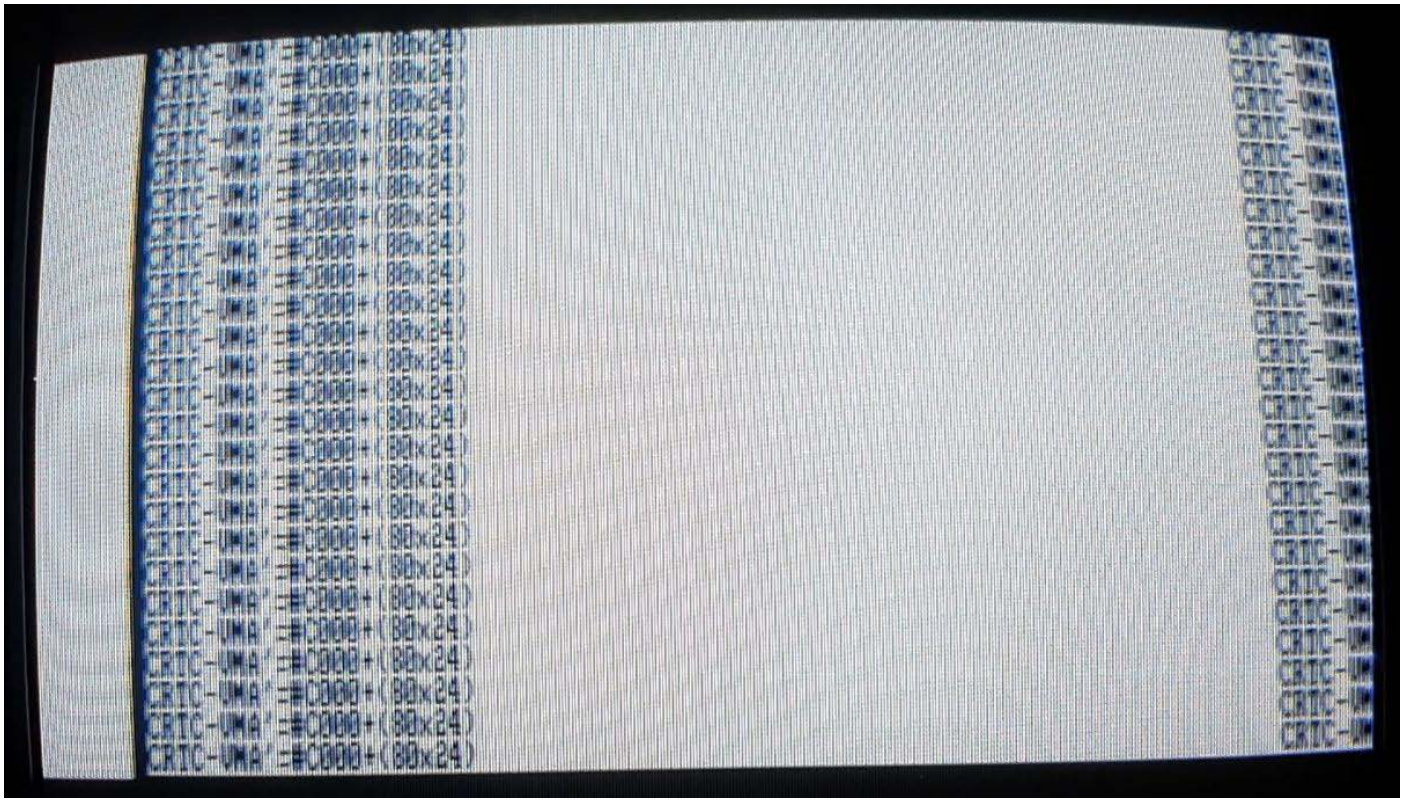
R1 STORIES

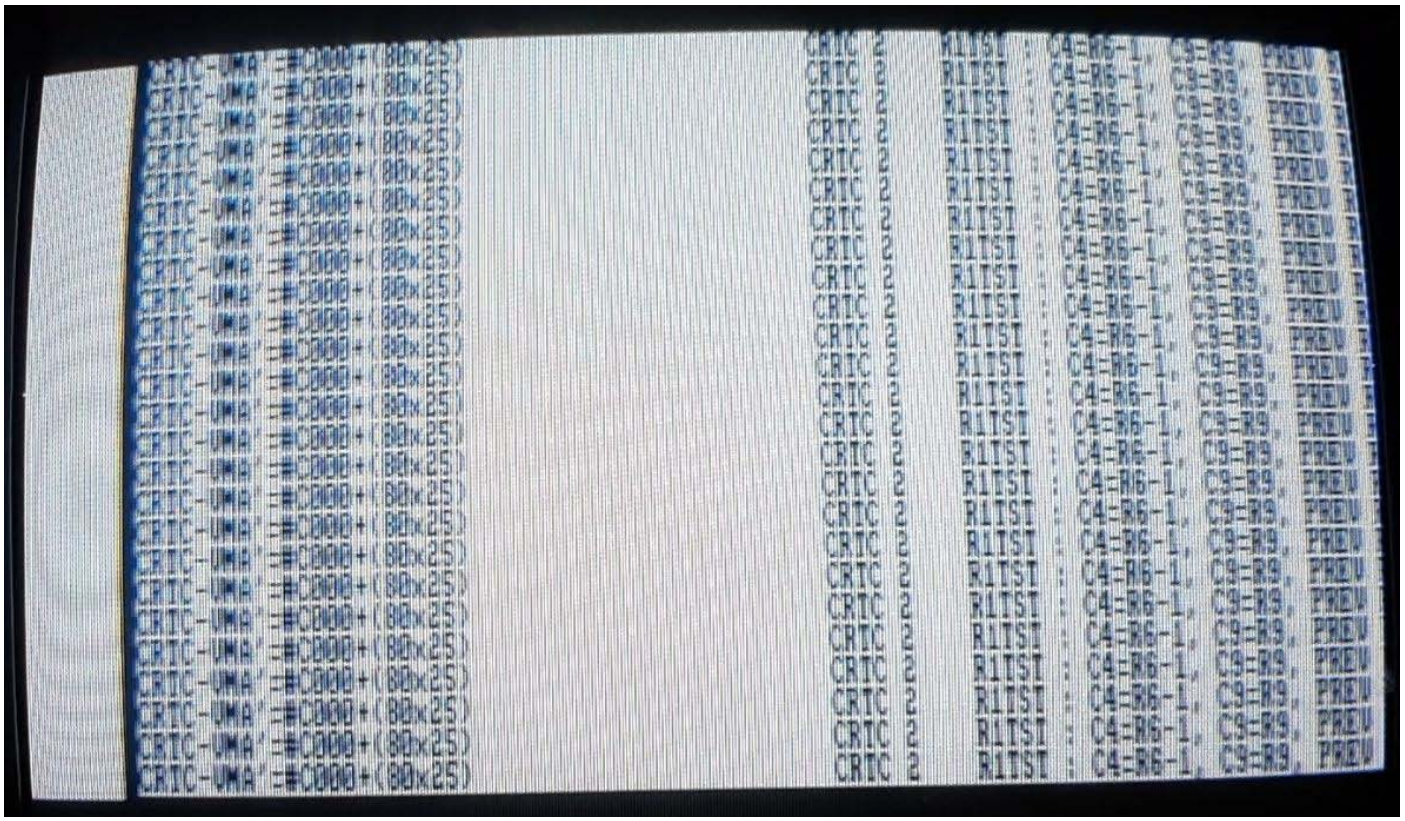
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(0) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

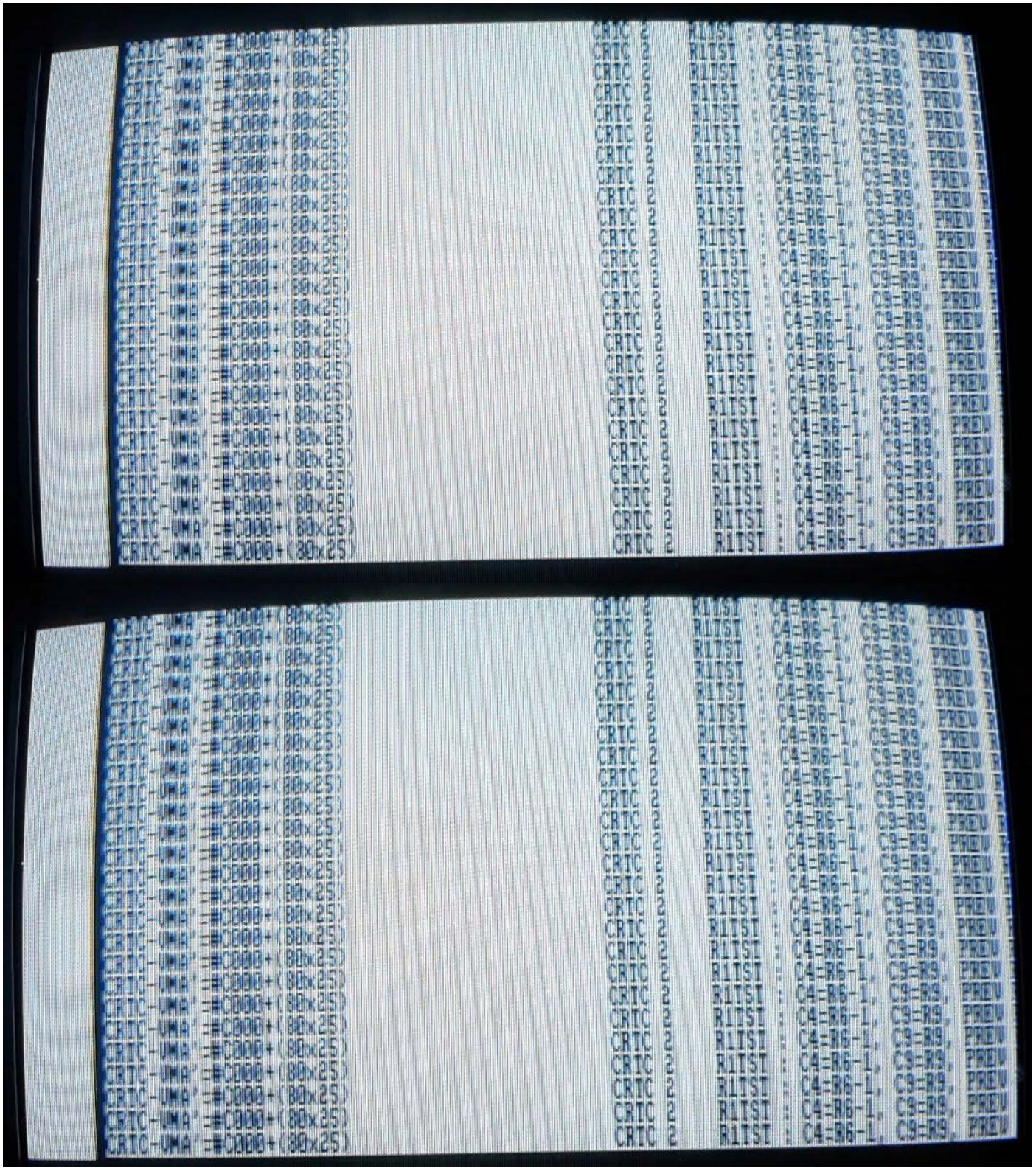



CRTC 2 R1 STORIES
STORY 2 : R1) R0 WHEN C9=R9 & C9()R9
PROCESS : UPDATE R1 ON 16 LINES (64 x 7, 40 (C9=7))+(40 x 7, 24(C9=7))
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27
(L1)AT #C000+(5x80)
(L2)AT #C000+(6x80))
(L2)AT #C000+(6x80))
(L3)AT #C000+(7x80))


CRTC 2 R1 STORIES
STORY 3 : R1=0 EFFECT (EACH LINE : 4 x OUT R1,0/OUT R1,40)
PROCESS : UPDATE R1=0 FOR 4x8 Lines FROM C0=3C, C0=3D, C0=3E, C0=3F
00 02 04 06 08 0A 0C 0E 10 12 14 16 18 1A 1C 1E 20 22 24 26
01 03 05 07 09 0B 0D 0F 11 13 15 17 19 1B 1D 1F 21 23 25 27

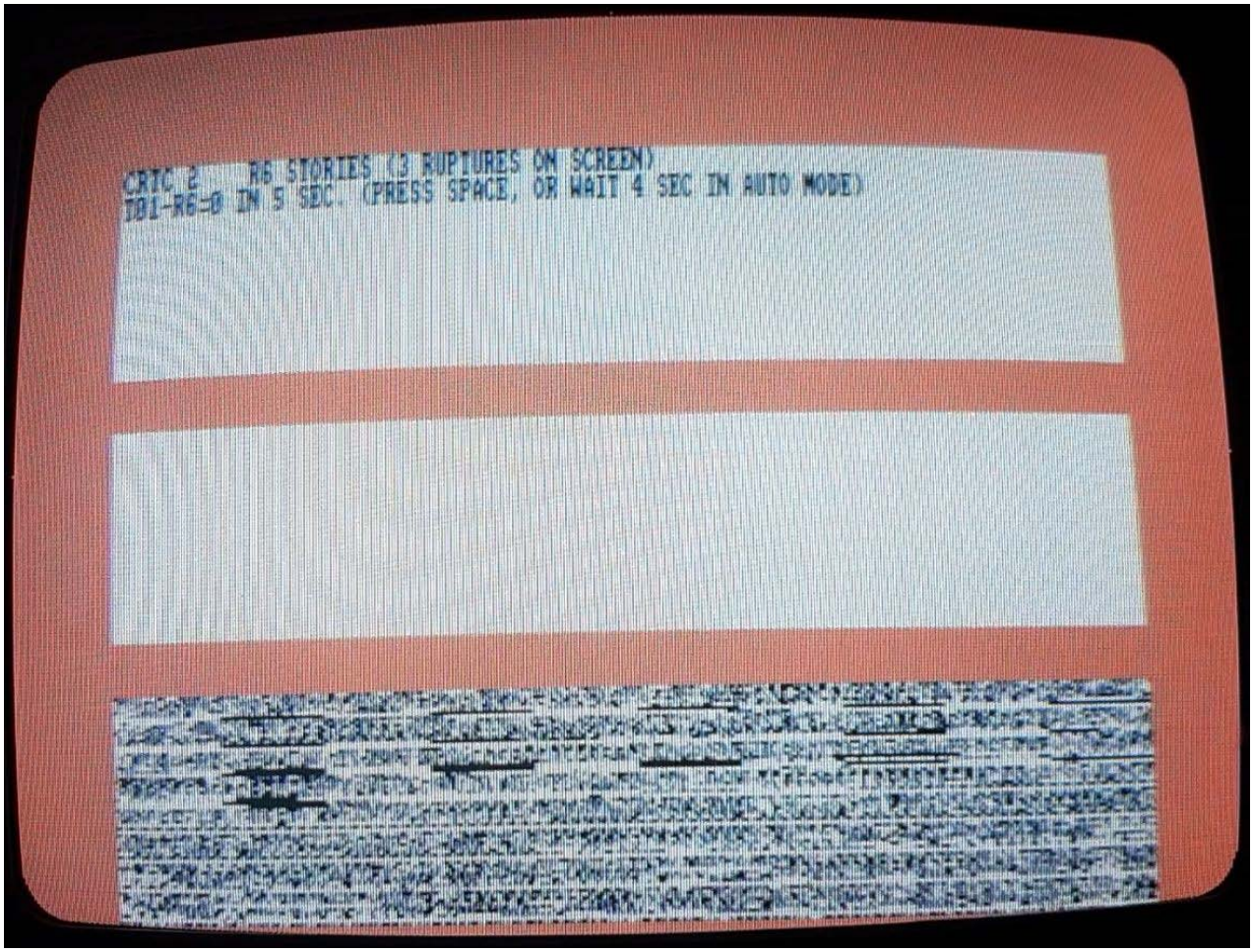


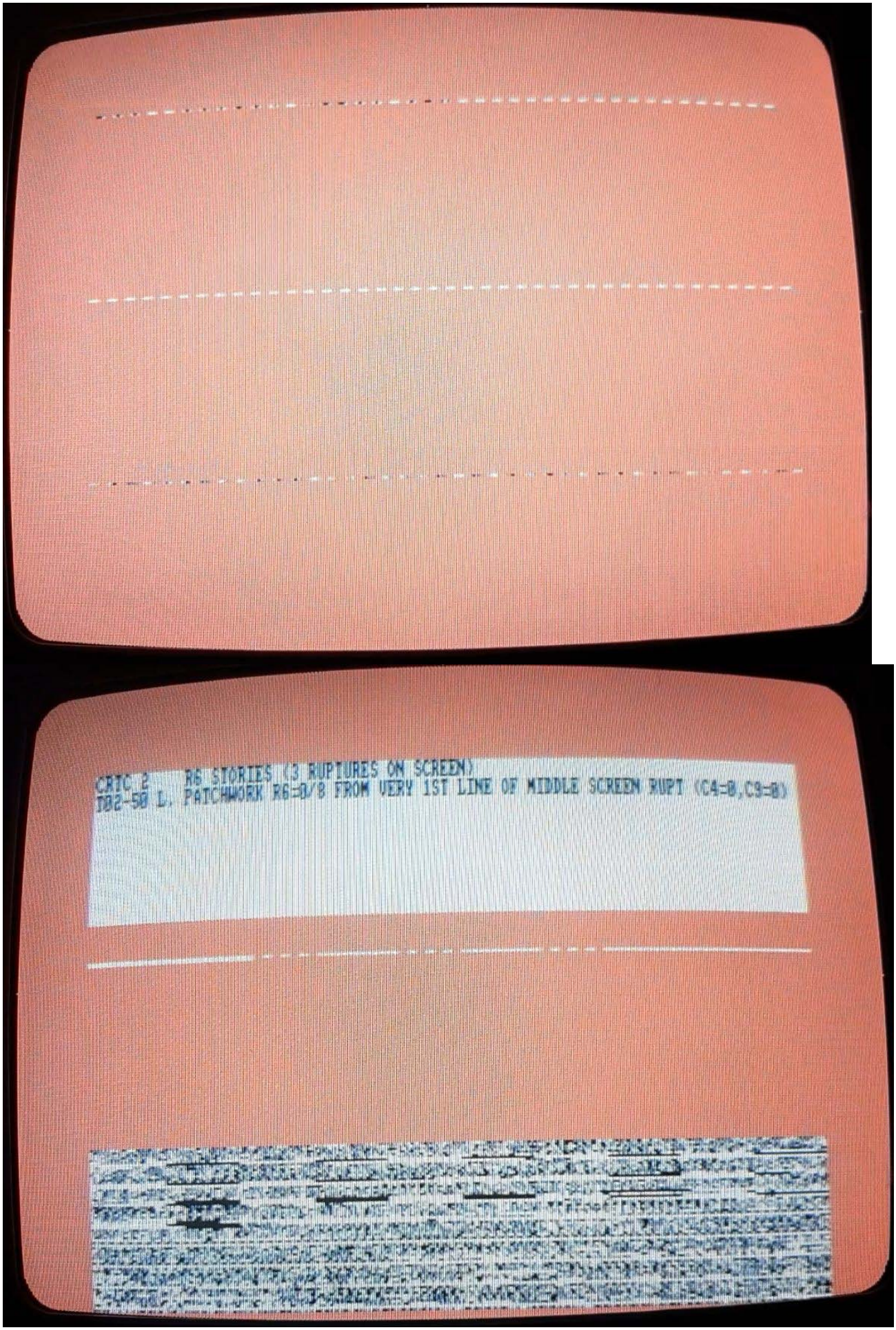


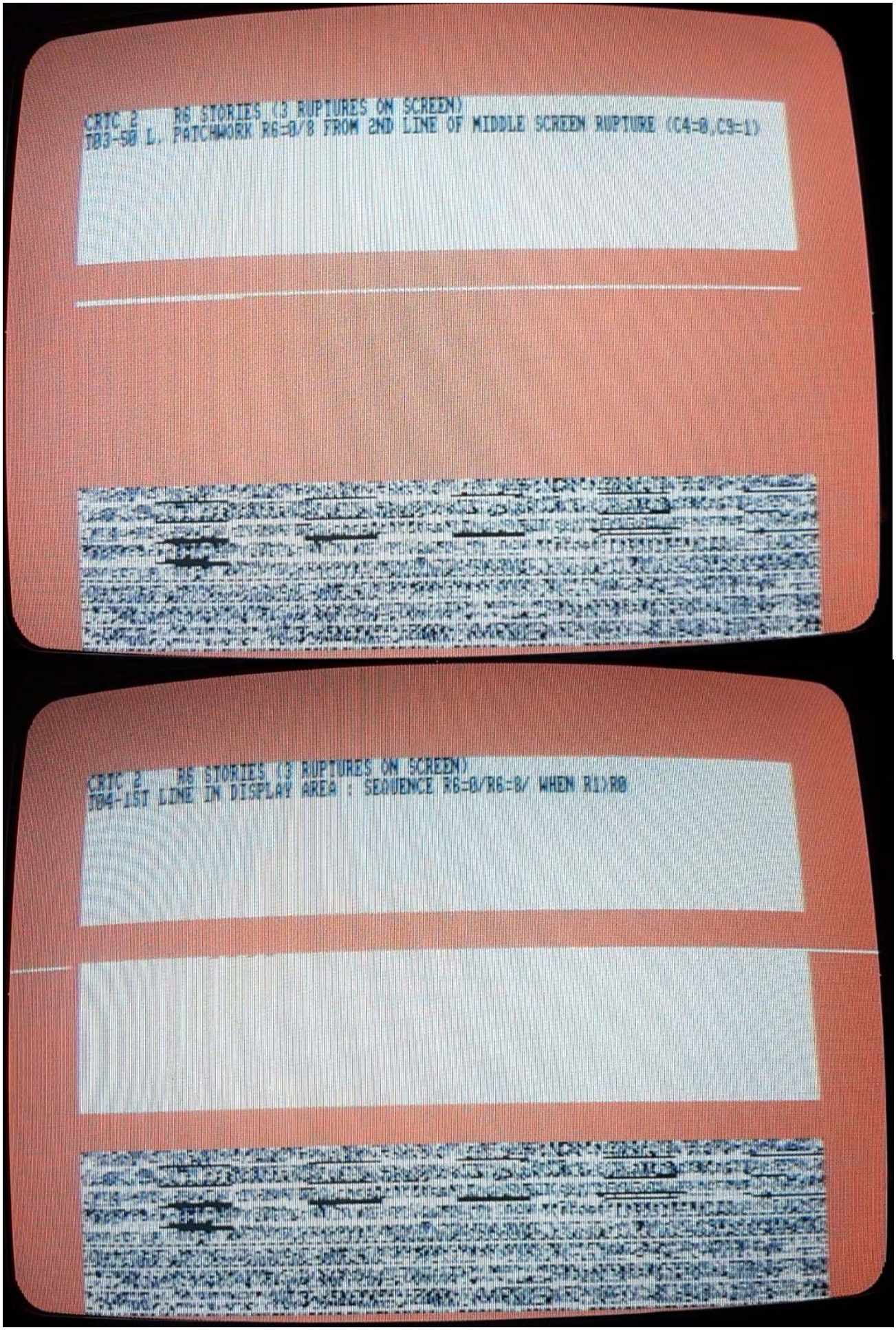


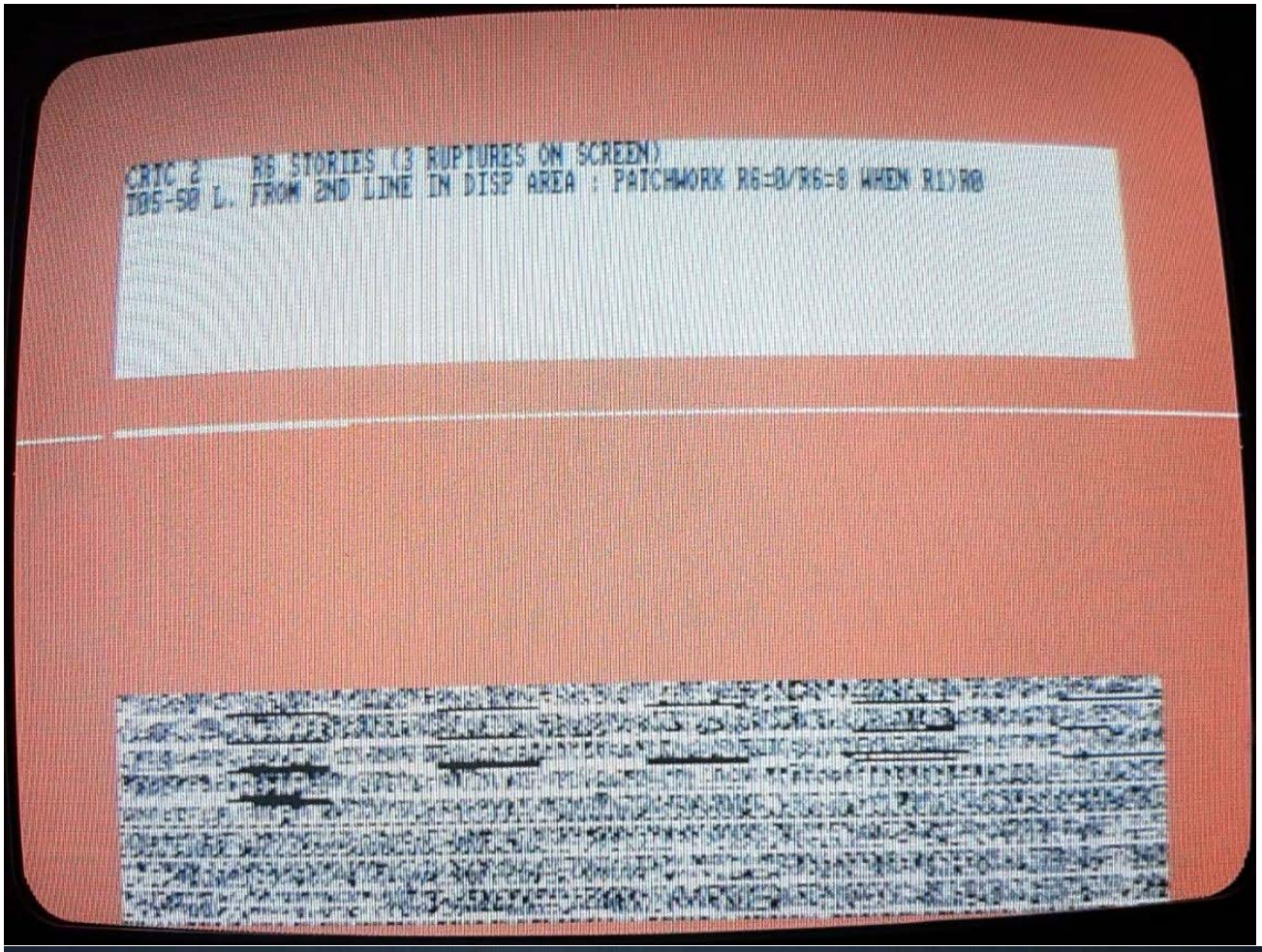
R6 STORIES

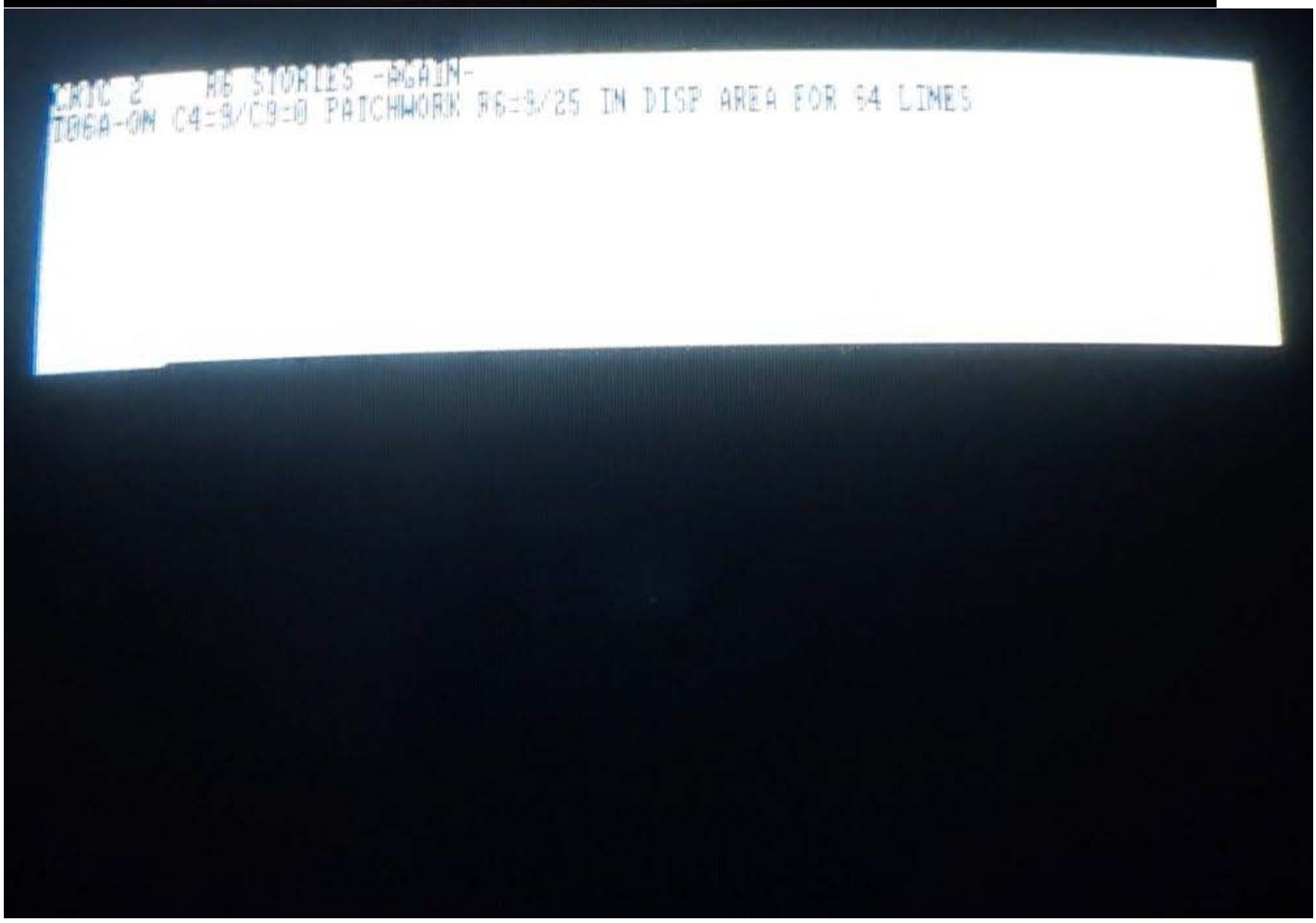
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

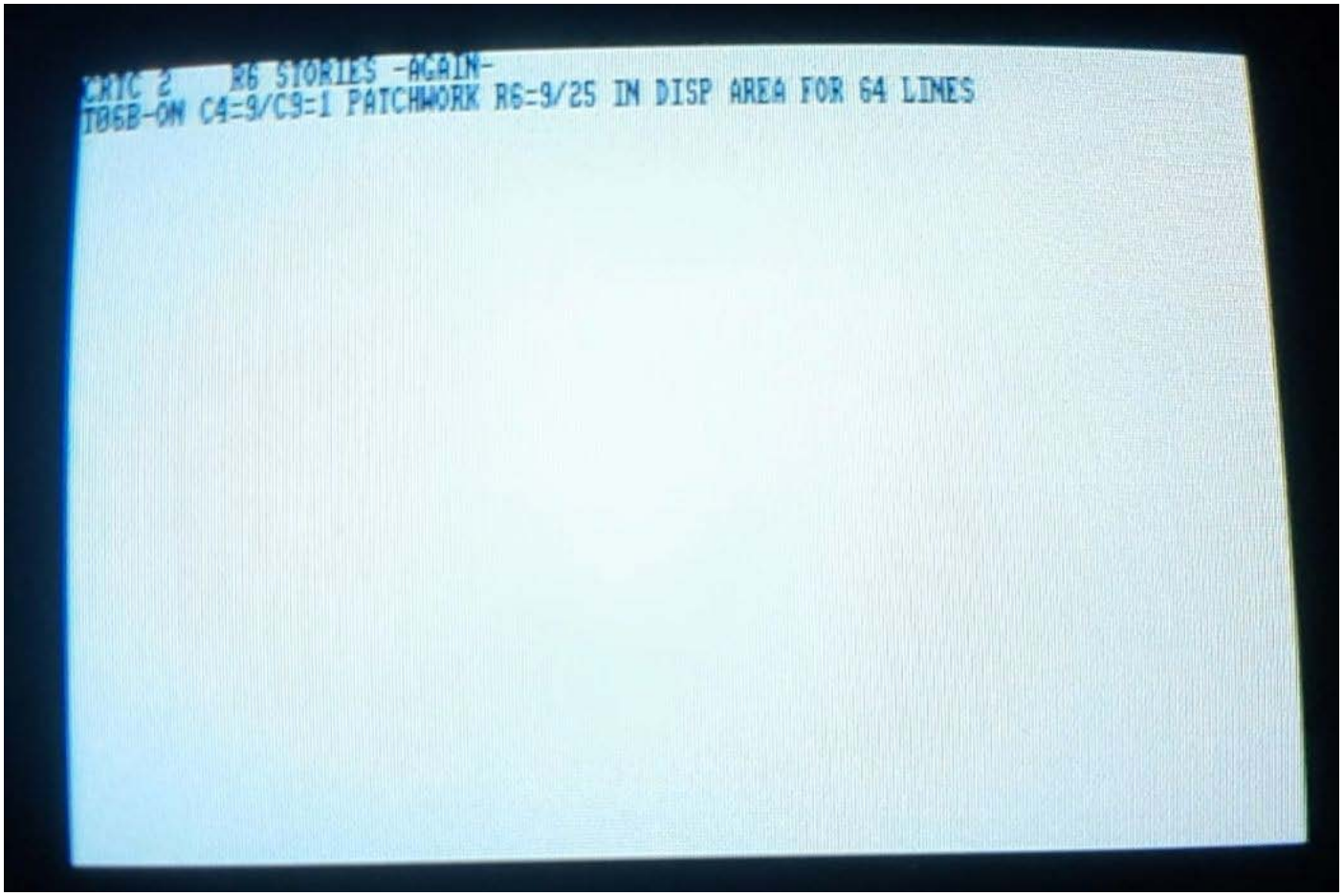


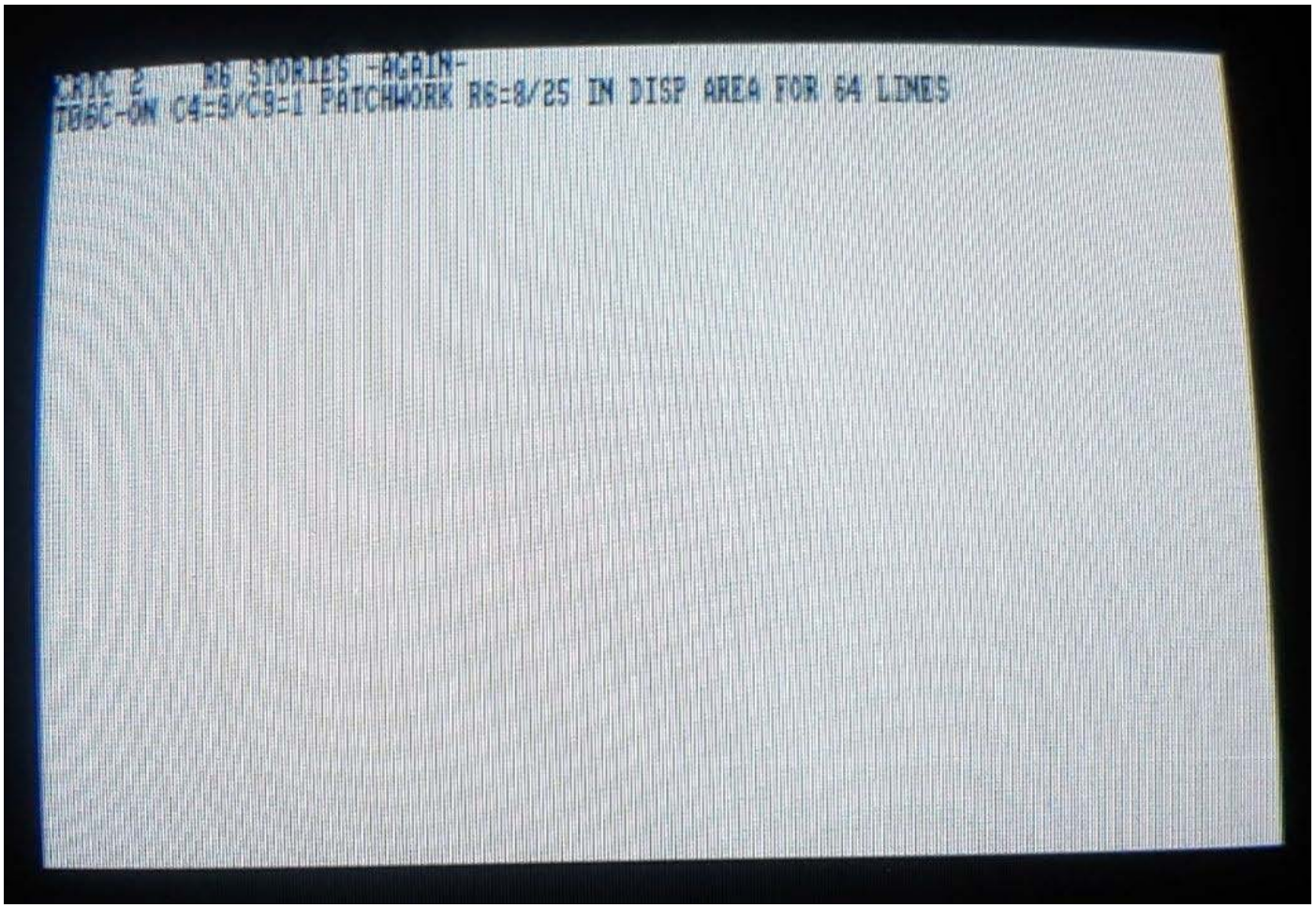

CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
IRQ-50 L. PATCHWORK R6=0/8 FROM VERY 1ST LINE OF MIDDLE SCREEN RUPT (C4=8,C9=8)

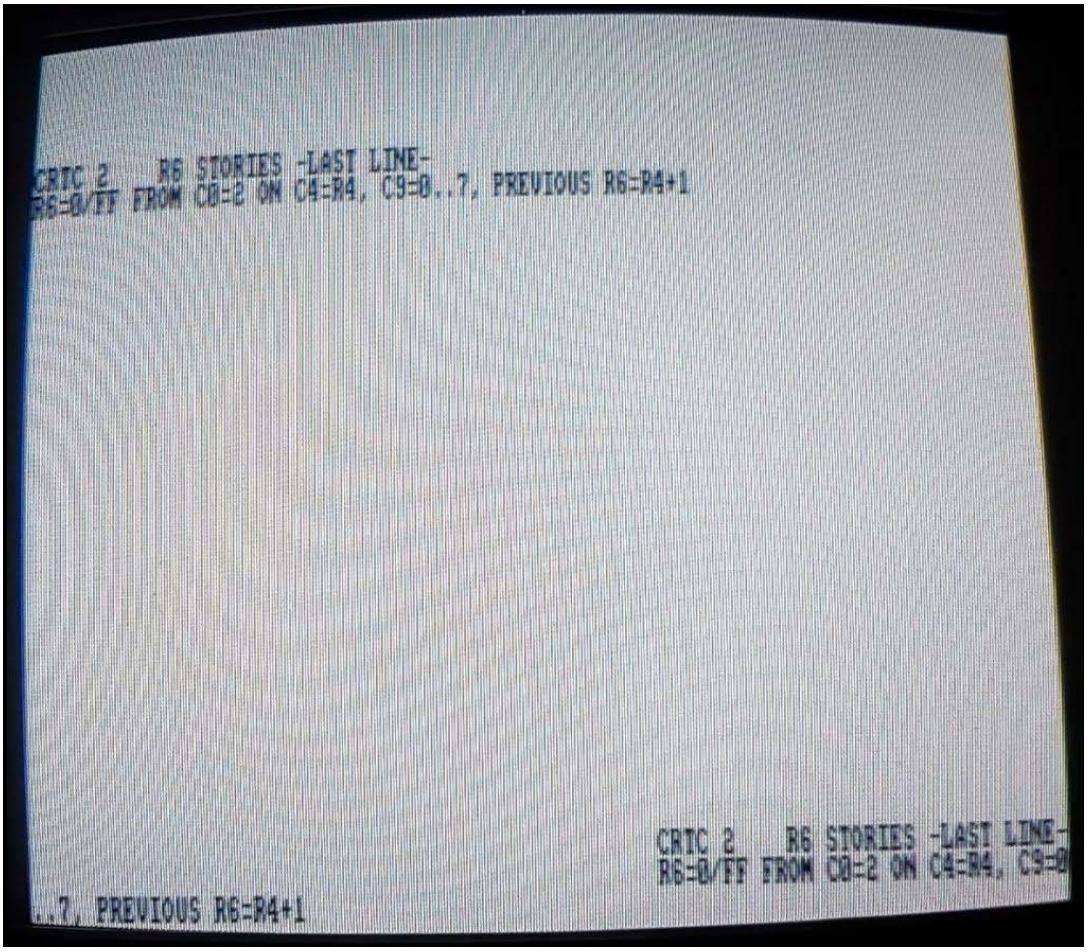

CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
1083-50 L. PATCHWORK R6=0/8 FROM 2ND LINE OF MIDDLE SCREEN RUPTURE (C4=0,C9=1)
CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
1084-1ST LINE IN DISPLAY AREA : SEQUENCE R6=0/R6=8/ WHEN R1)R0

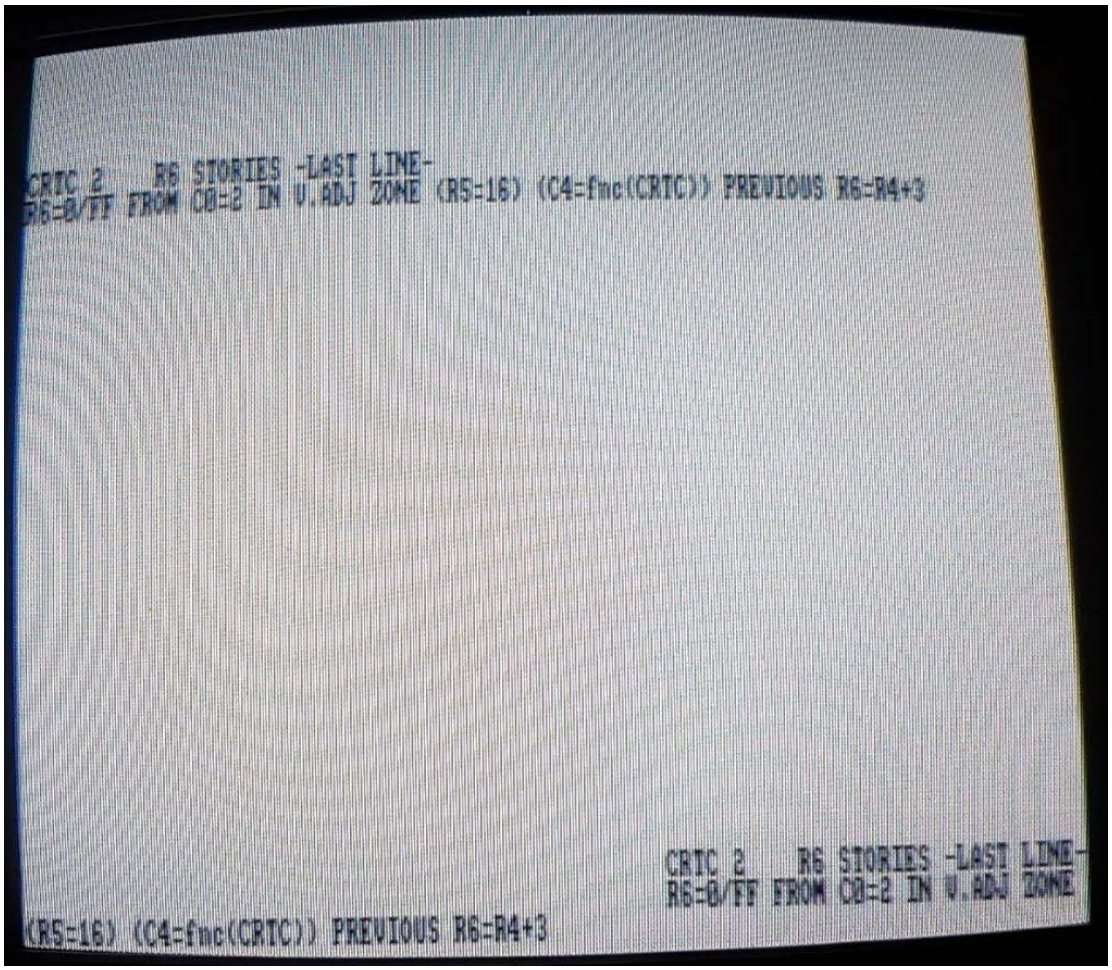

CRTC 2 R6 STORIES (3 RUPTURES ON SCREEN)
TOS-50 L. FROM 2ND LINE IN DISP AREA : PATCHWORK R6=0/R6=8 WHEN R1/R0

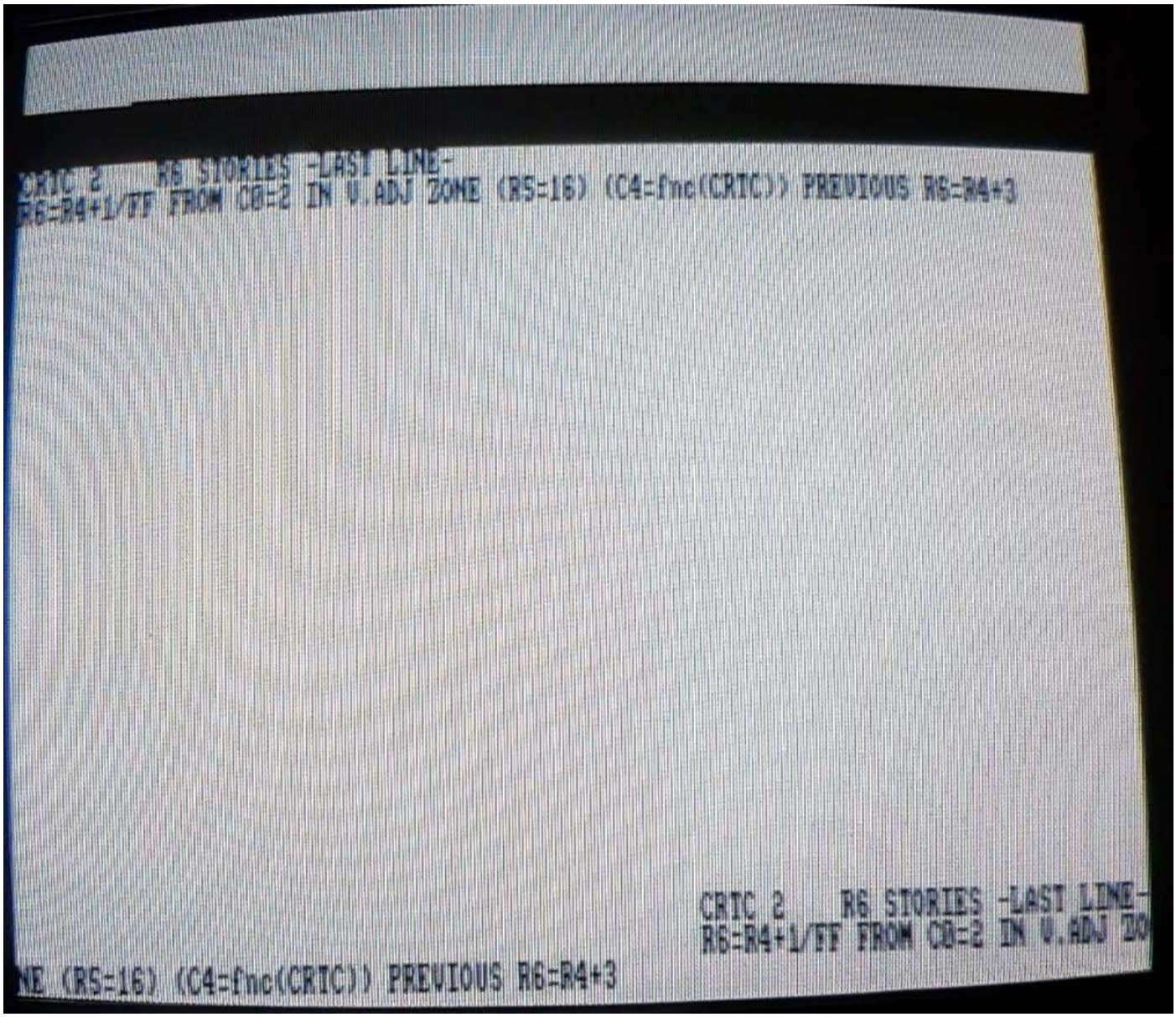

CRTC 2 R6 STORIES -AGAIN-
IDEA-OM C4=9/C9=0 PATCHWORK R6=9/25 IN DISP AREA FOR 54 LINES


R6 STORIES -AGAIN-
IBGB-ON C4=9/C9=1 PATCHWORK R6=9/25 IN DISP AREA FOR 64 LINES


R6 STORIES -AGAIN-
IBGB-ON C4=9/C9=1 PATCHWORK R6=8/25 IN DISP AREA FOR 64 LINES


CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 ON C4=R4, C9=0..7, PREVIOUS R6=R4+1
CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 ON C4=R4, C9=0
..7, PREVIOUS R6=R4+1


CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 IN V.ADJ ZONE (R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3
CRTC 2 R6 STORIES -LAST LINE-
R6=0/FF FROM C0=2 IN V.ADJ ZONE
(R5=16) (C4=fnc(CRTC)) PREVIOUS R6=R4+3


CRIC 2 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM C6=2 IN V.ADJ ZONE (R5=16) (C4=fnc(CRIC)) PREVIOUS R6=R4+3
CRIC 2 R6 STORIES -LAST LINE-
R6=R4+1/FF FROM C6=2 IN V.ADJ ZO
NE (R5=16) (C4=fnc(CRIC)) PREVIOUS R6=R4+3

RVNI (NON INVISIBLE VERTICAL RUPTURE)

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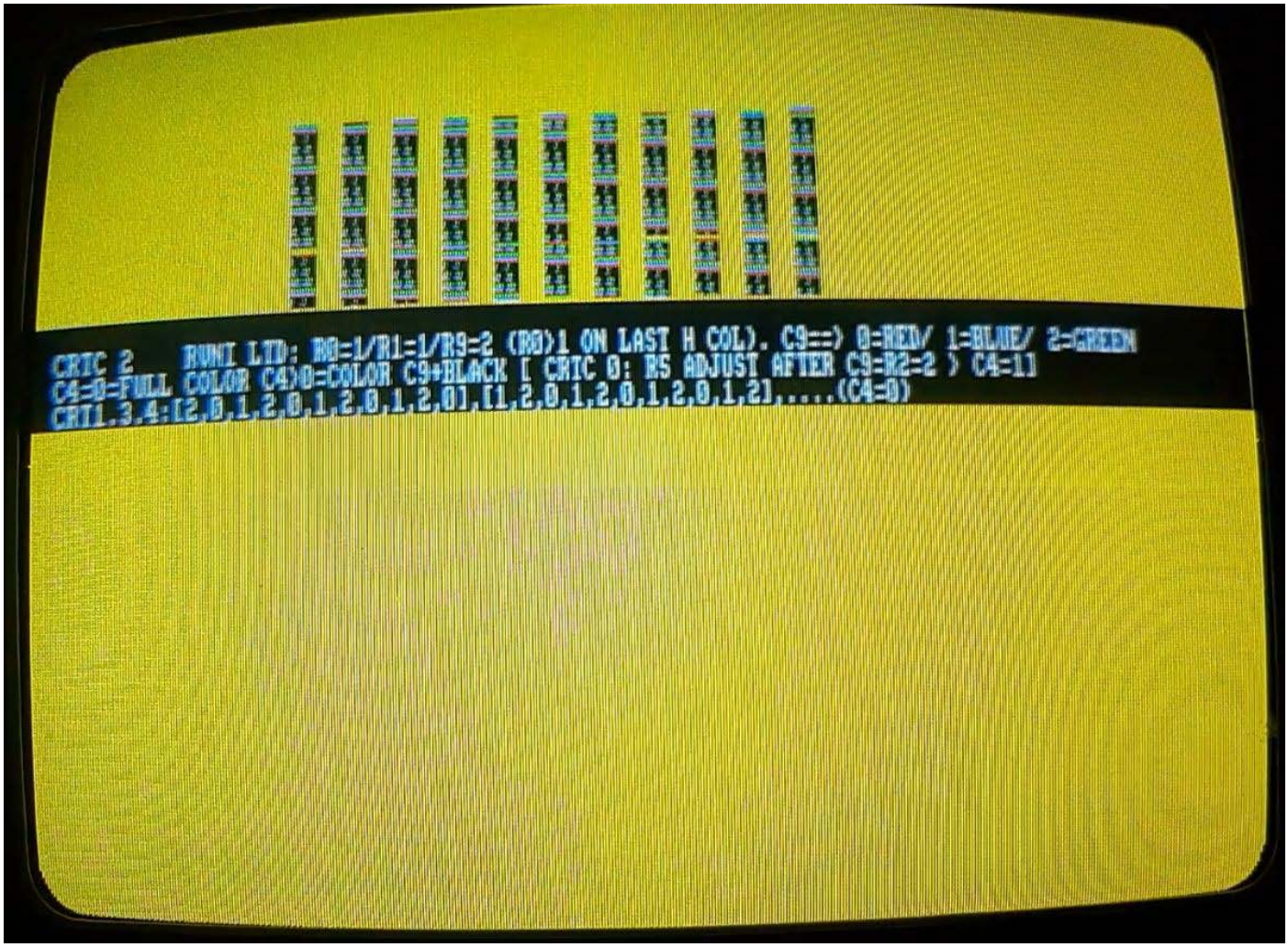
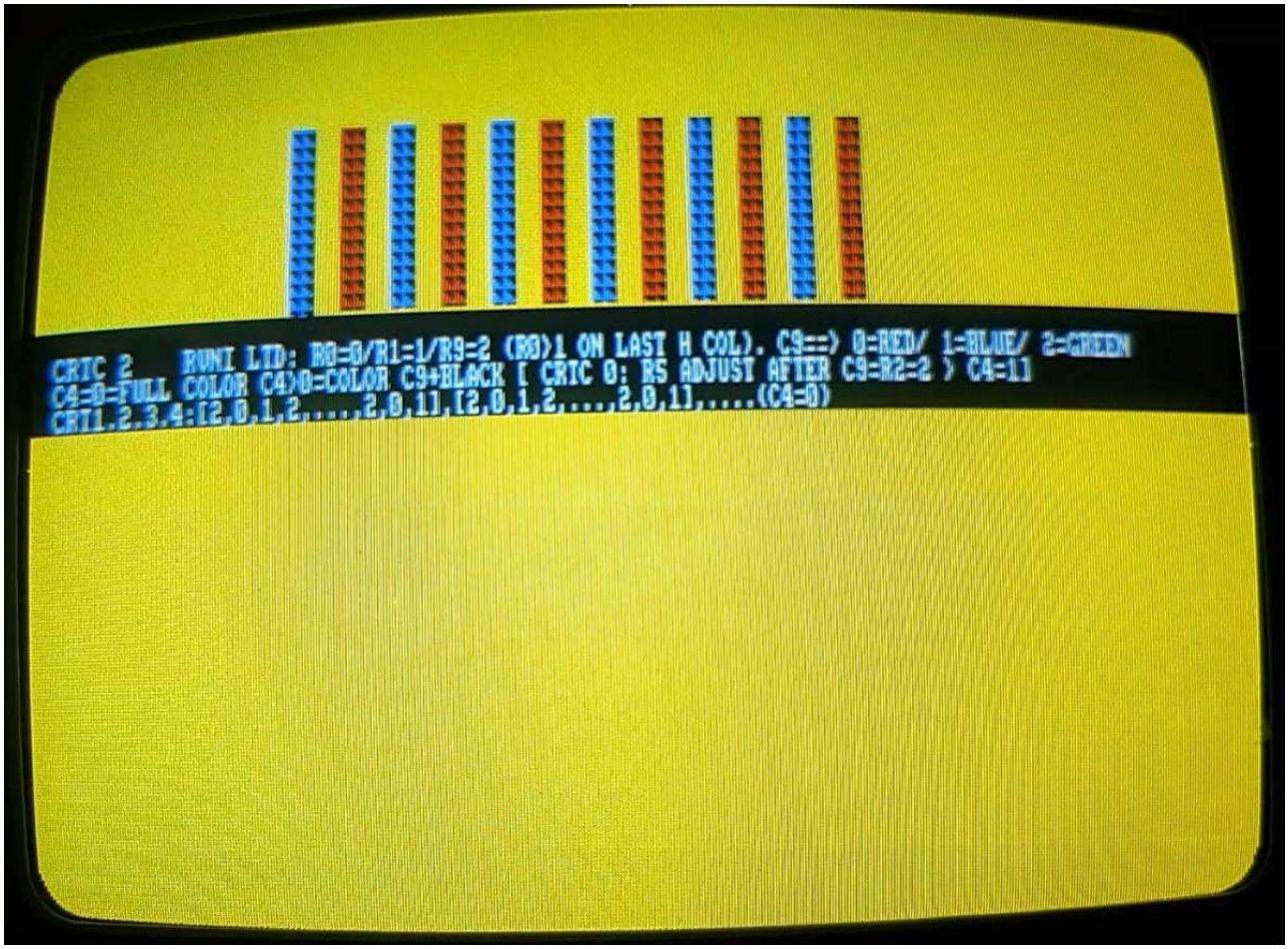
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



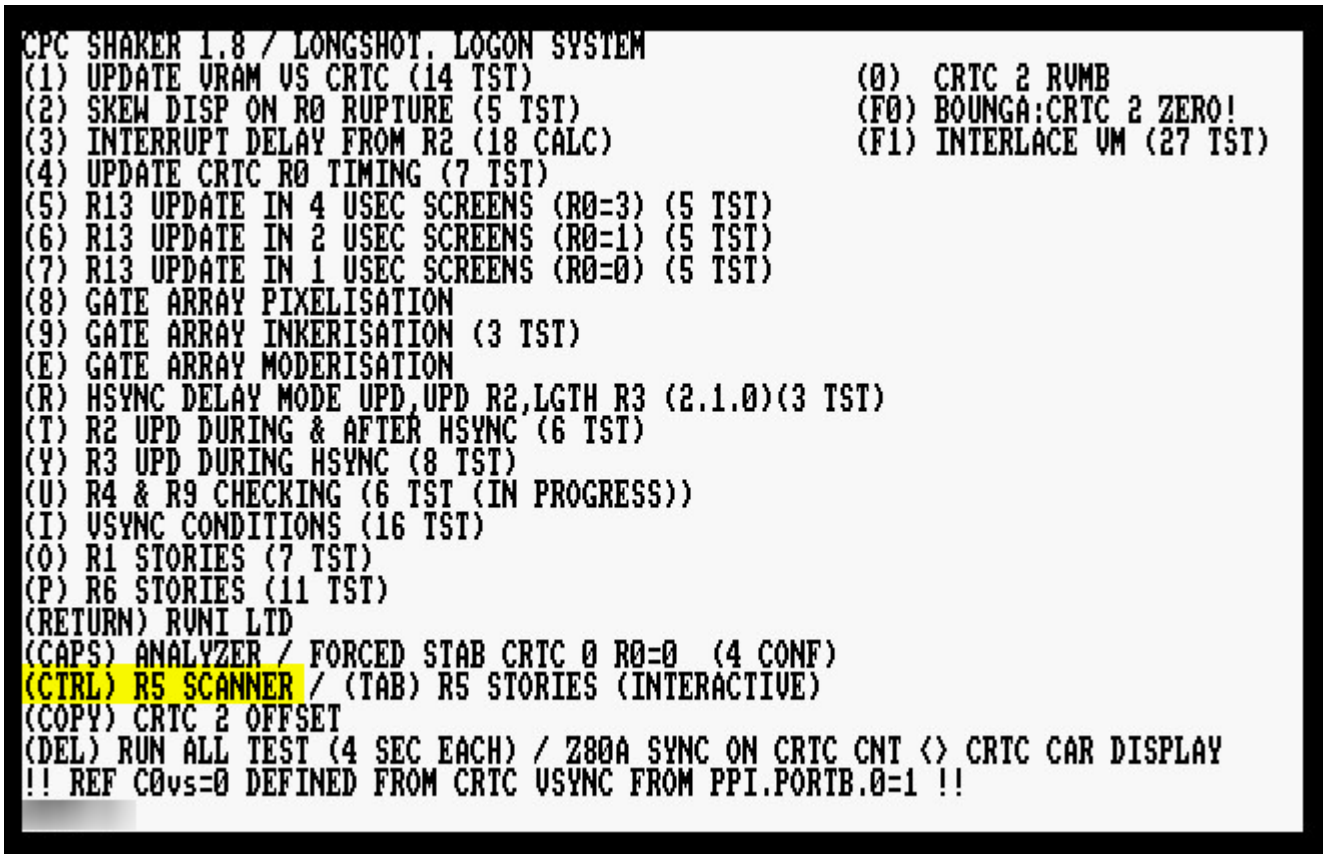

CRTC 2 RUNI LTD: R0=0/R1=1/R9=2 (R0)1 ON LAST H COL). C9==) 0=RED/ 1=BLUE/ 2=GREEN
C4=0=FULL COLOR C4)0=COLOR C9+BLACK [CRTC 0: RS ADJUST AFTER C9=R2=2) C4=1]
CRT1.2.3.4:[2,0,1,2,...,2,0,1],[2,0,1,2,...,2,0,1],....(C4=0)


CRTC 2 RUNI LTD: R0=0/R1=1/R9=2 (R0)1 ON LAST H COL). C9==) 0=RED/ 1=BLUE/ 2=GREEN
C4=0=FULL COLOR C4)0=COLOR C9+BLACK [CRTC 0: RS ADJUST AFTER C9=R2=2) C4=1]
CRT1.2.3.4:[2,0,1,2,...,2,0,1],[2,0,1,2,...,2,0,1],....(C4=0)

ANALYZER / FORCED STABILISATION ON R0=0

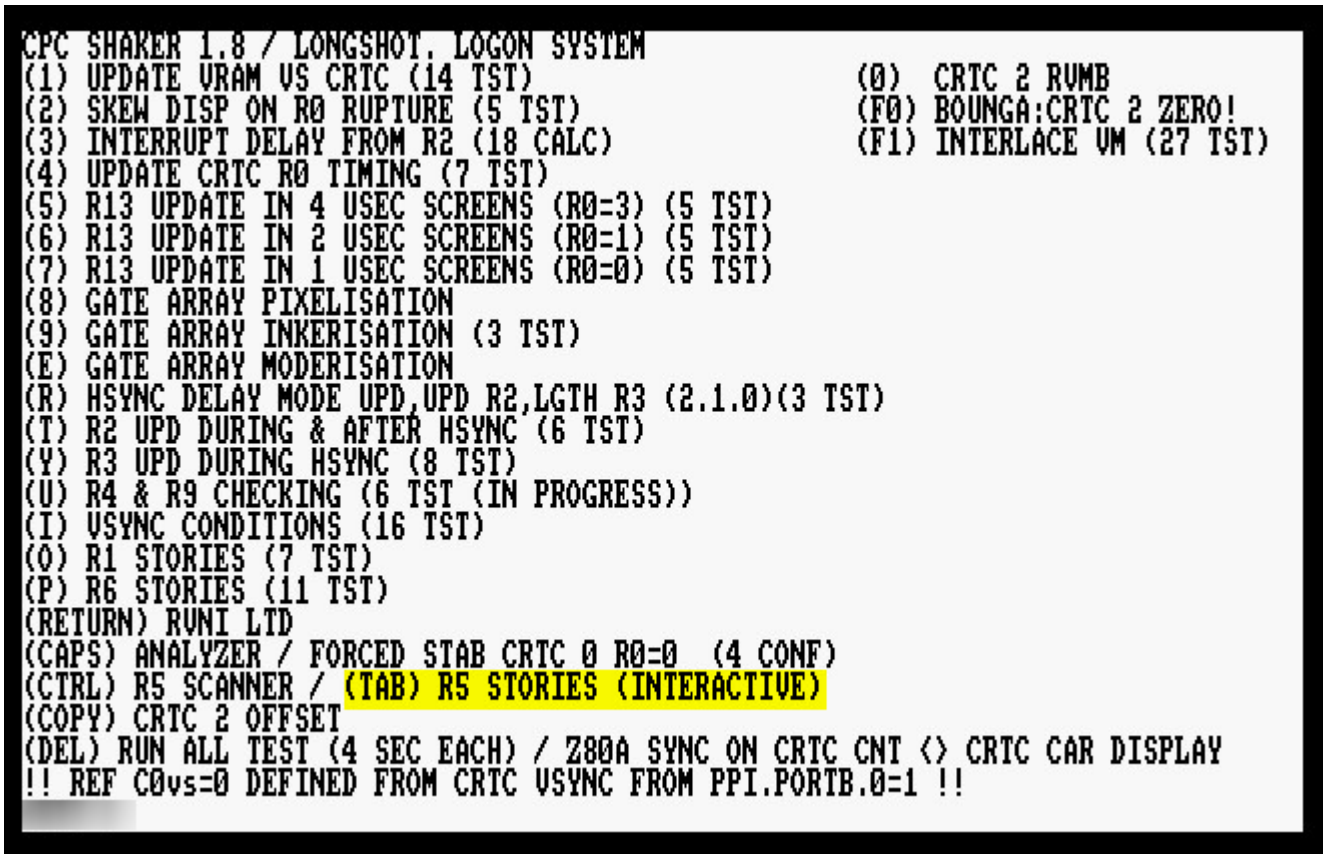
```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```

R5 SCANNER (for CRTC 1)



Only for CRTC 1

R5 STORIES / INTERACTIVE TEST



Only for CRTC 1

OFFSET UPDATE

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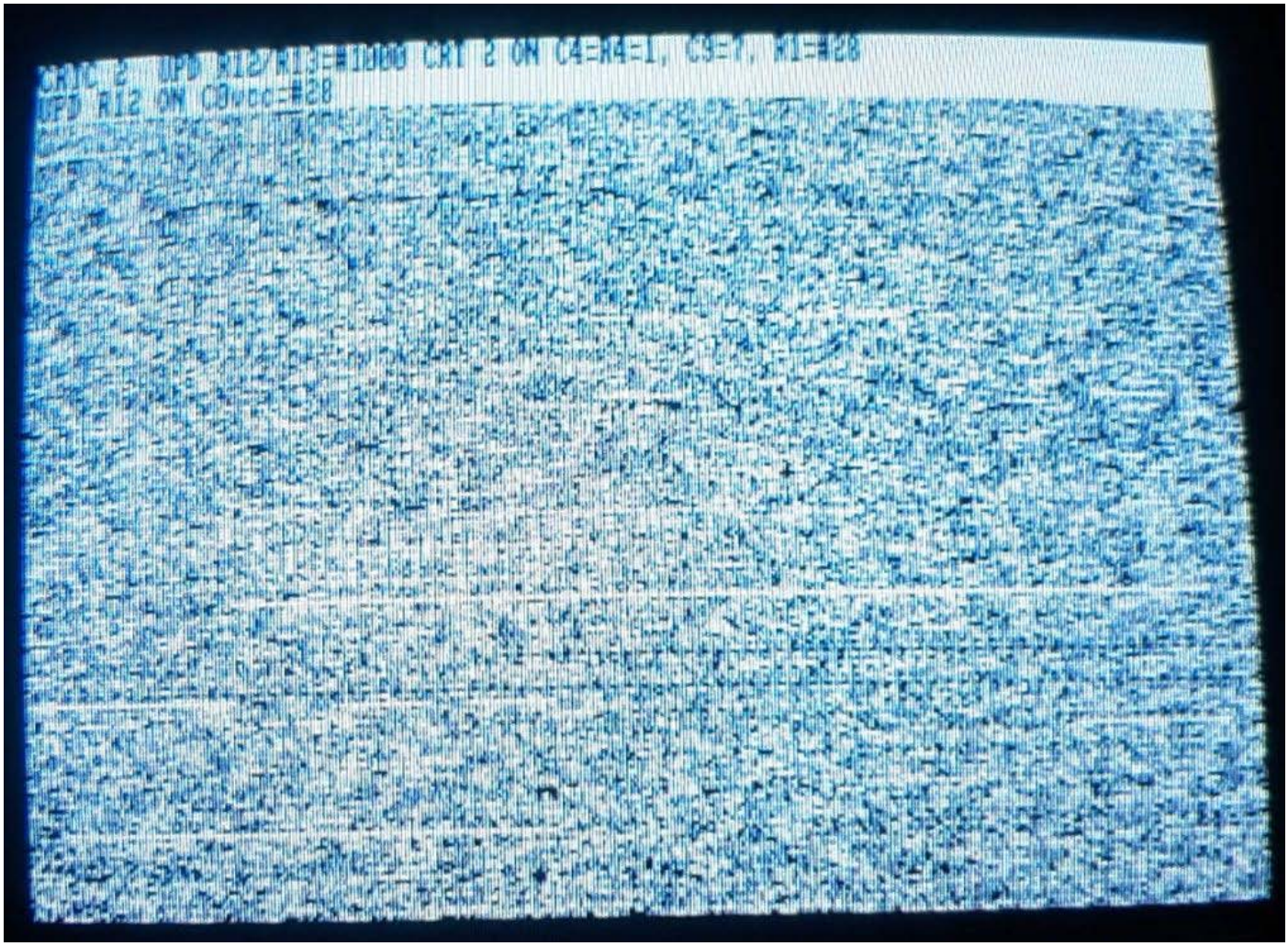
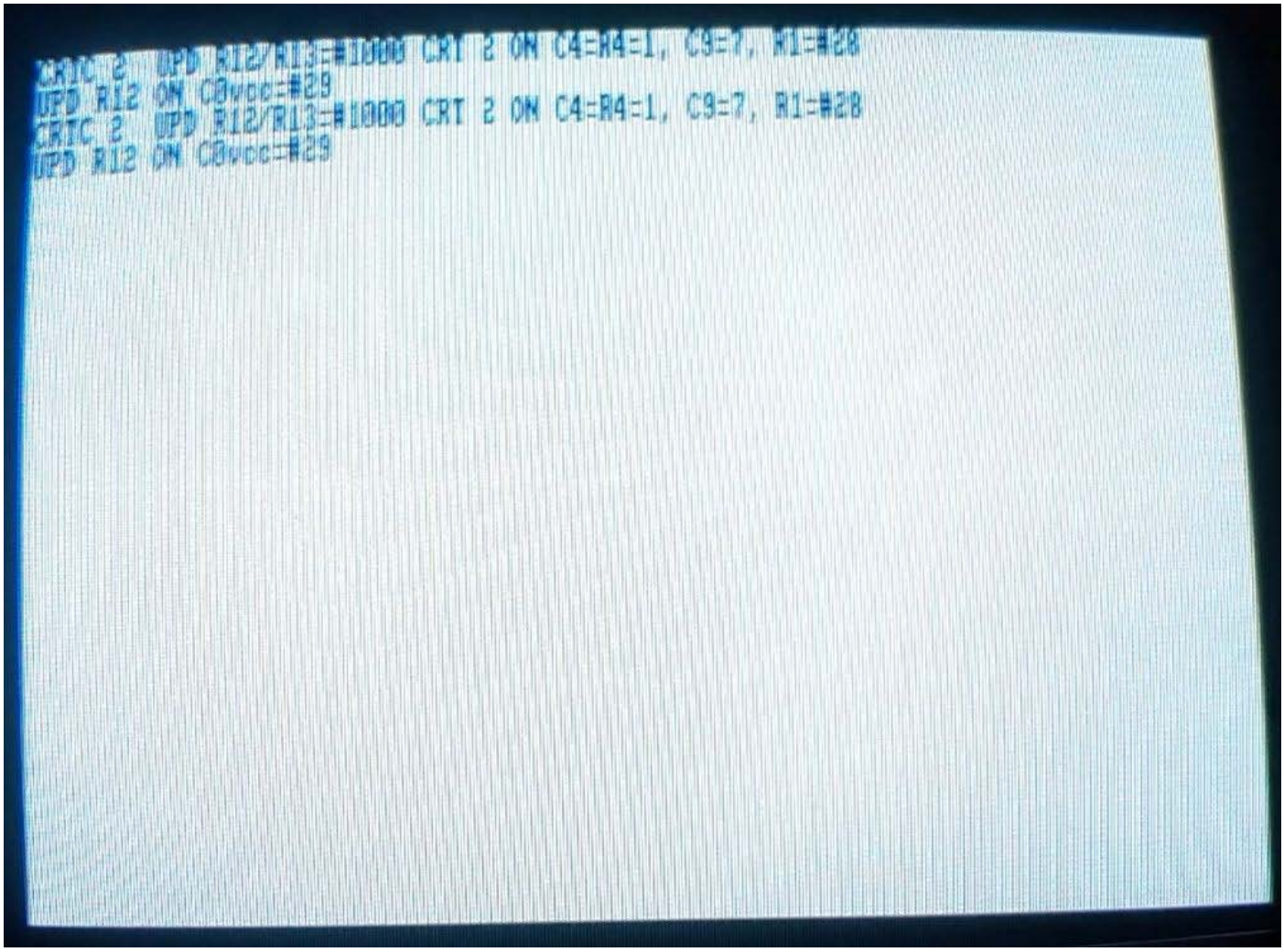
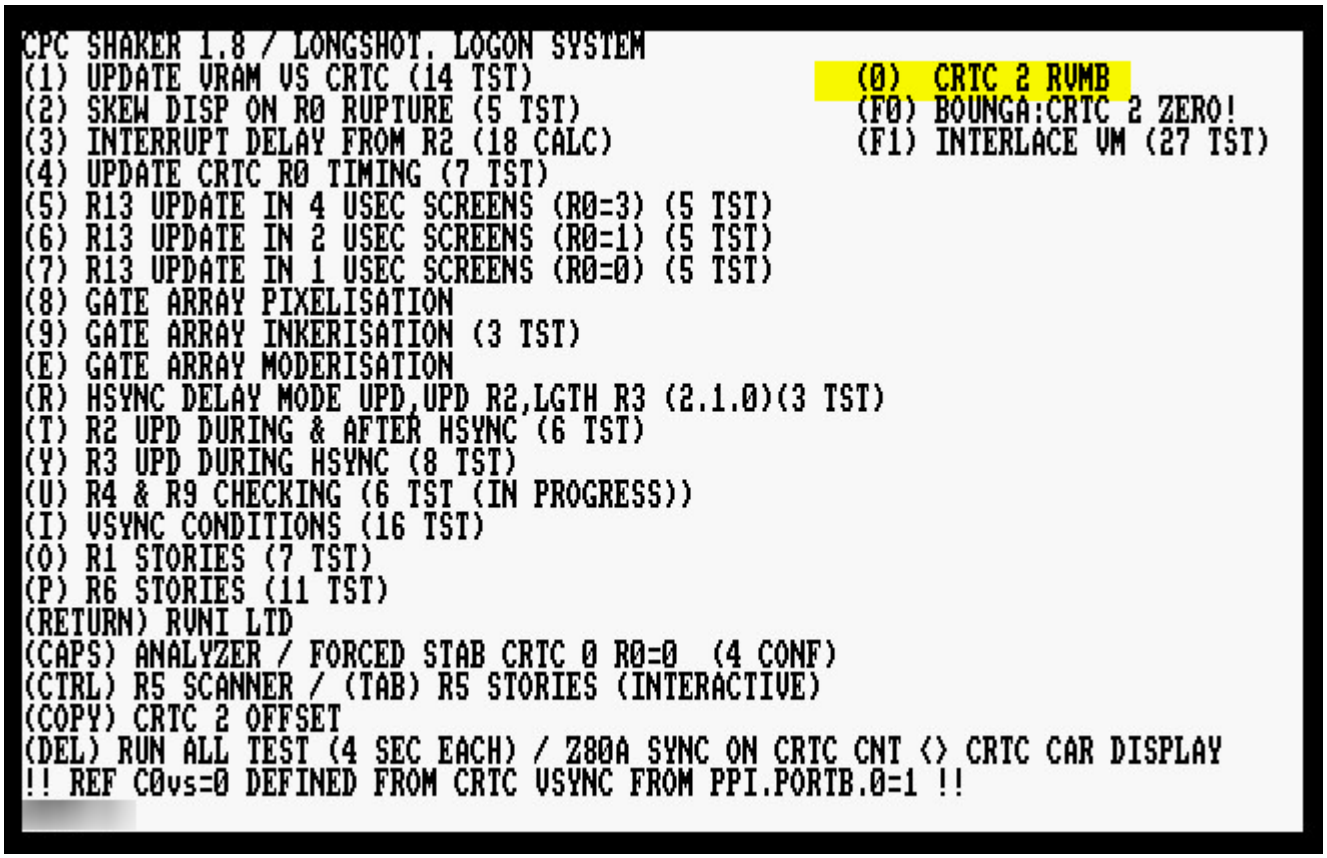
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



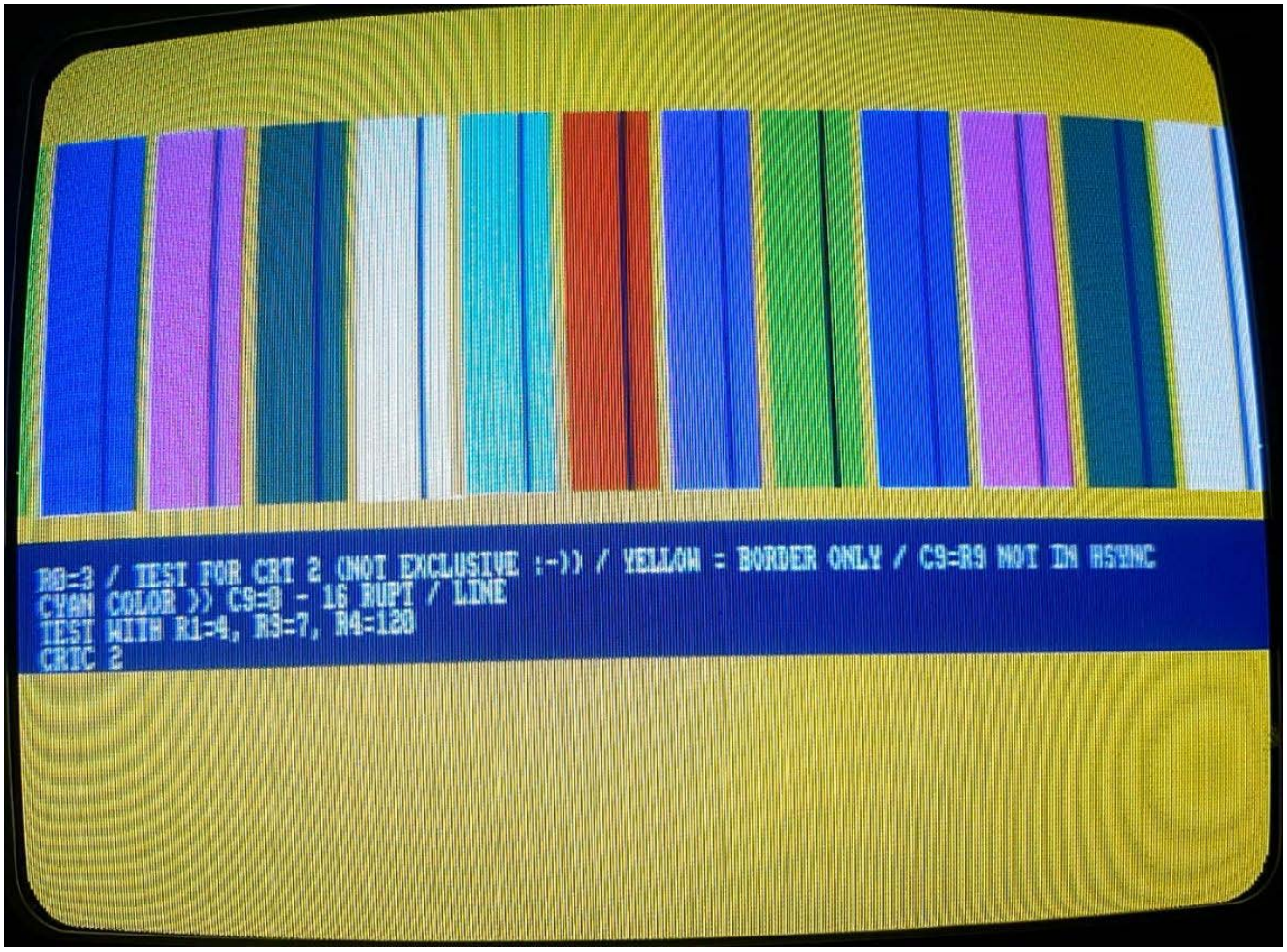

CRTC 2 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON C0vcc=#29
CRTC 2 UPD R12/R13=#1000 CRT 2 ON C4=R4=1, C9=7, R1=#28
UPD R12 ON C0vcc=#29

« RVMB »


CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)
(2) SKEW DISP ON R0 RUPTURE (5 TST)
(3) INTERRUPT DELAY FROM R2 (18 CALC)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0 (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
(0) CRTC 2 RVMB
(F0) BOUNGA:CRTC 2 ZERO!
(F1) INTERLACE VM (27 TST)


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 16 RUPT / LINE
TEST WITH R1=3, R9=7, R4=120
CRTC 2


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 16 RUPT / LINE
TEST WITH R1=3, R9=7, R4=120
CRTC 2


R0=3 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 16 BUPI / LINE
TEST WITH R1=4, R9=7, R4=120
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 BUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 BUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=0
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 NUPI / LINE
TEST WITH R1=1, R9=7, R4=120
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 NUPI / LINE
TEST WITH R1=1, R9=7, R4=120
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=120
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=1, R9=7, R4=120
CRTC 2


R9=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=128
CRTC 2


R9=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=128
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=128
CRTC 2


R0=1 / TEST FOR CRT 2 (NOT EXCLUSIVE :-)) / YELLOW = BORDER ONLY / C9=R9 NOT IN HSYNC
CYAN COLOR)) C9=0 - 32 RUPT / LINE
TEST WITH R1=2, R9=7, R4=128
CRTC 2

BOUNGA : CRTC 2 R4=R9=0 FORCED

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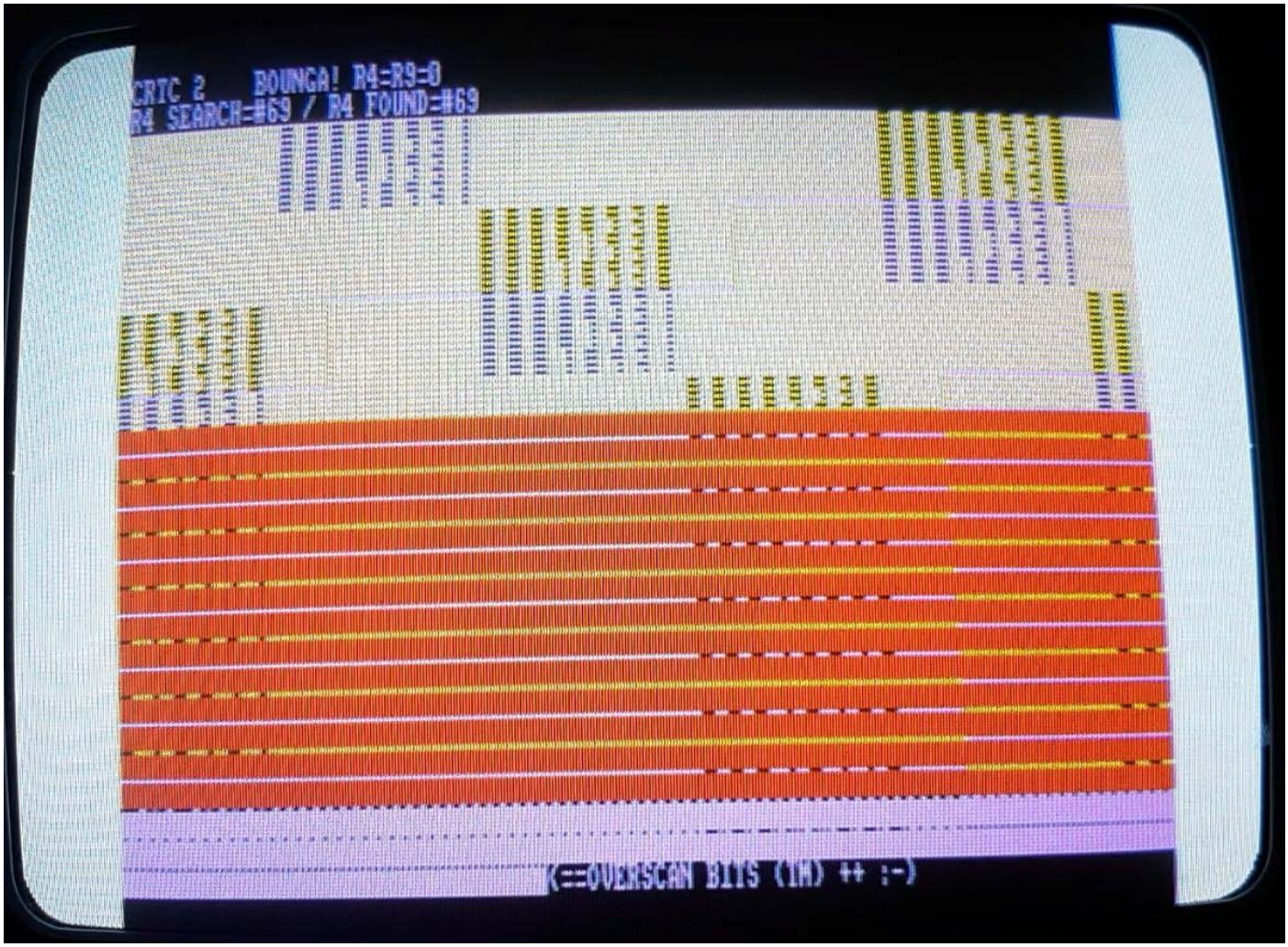
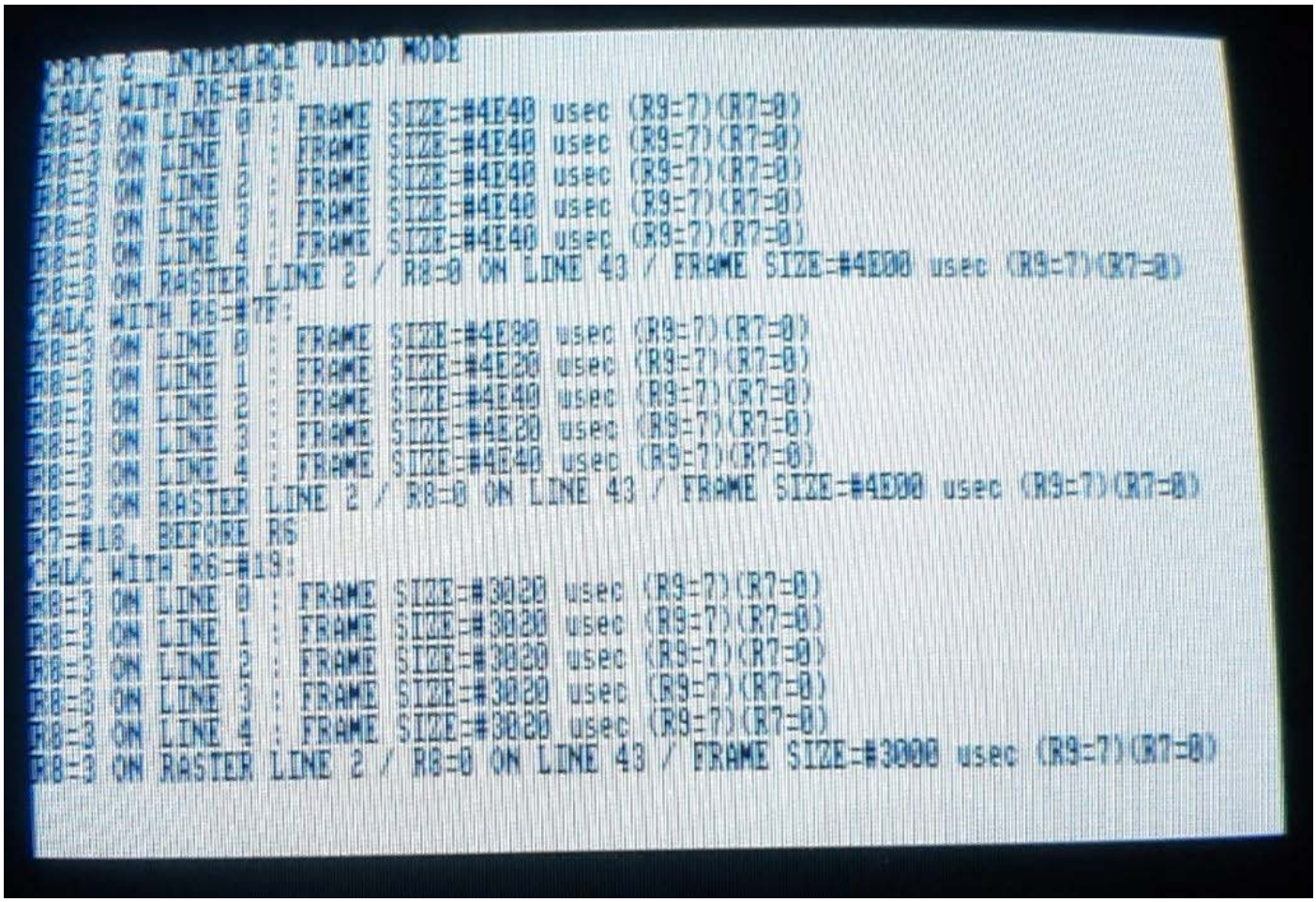
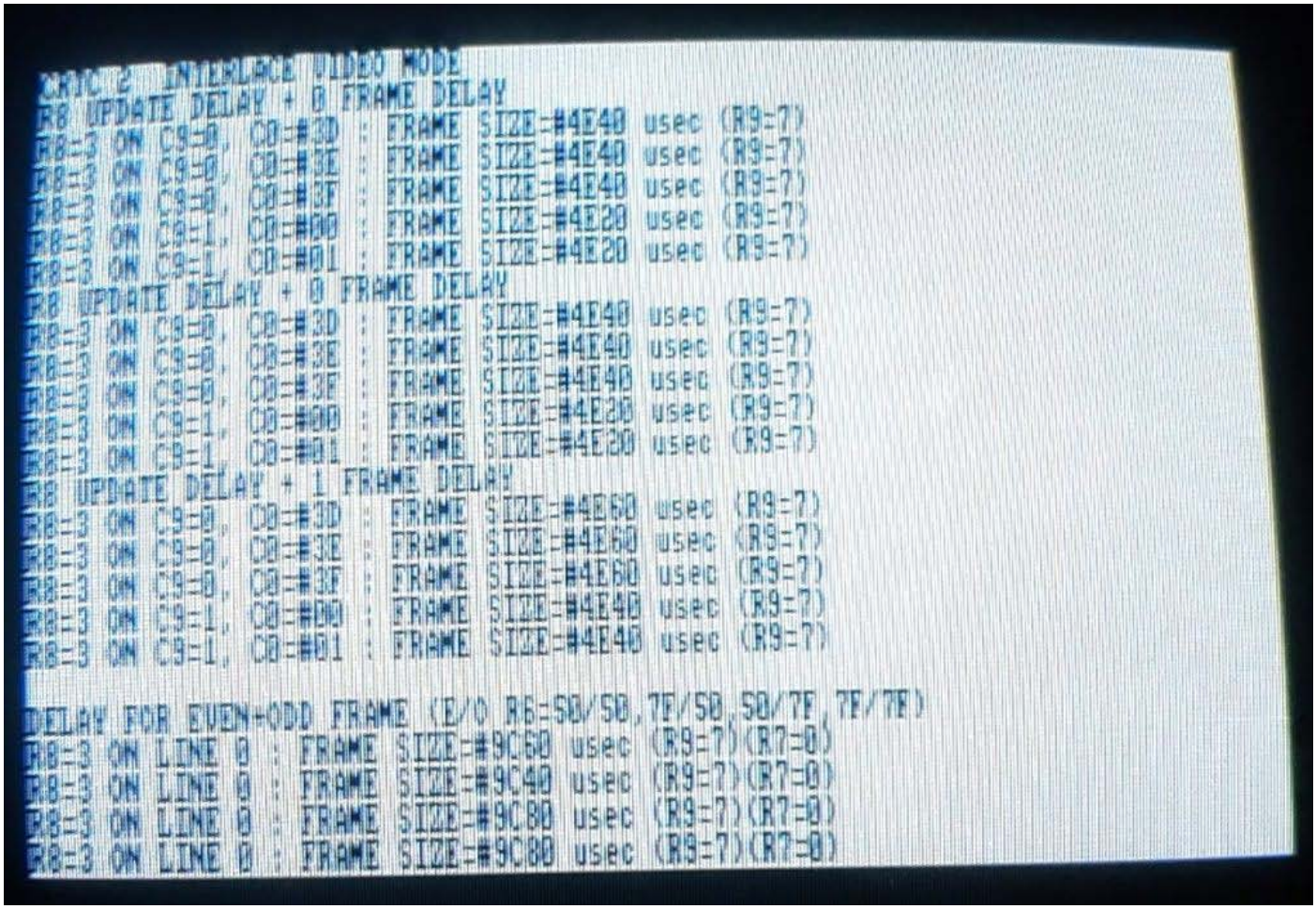
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RVNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



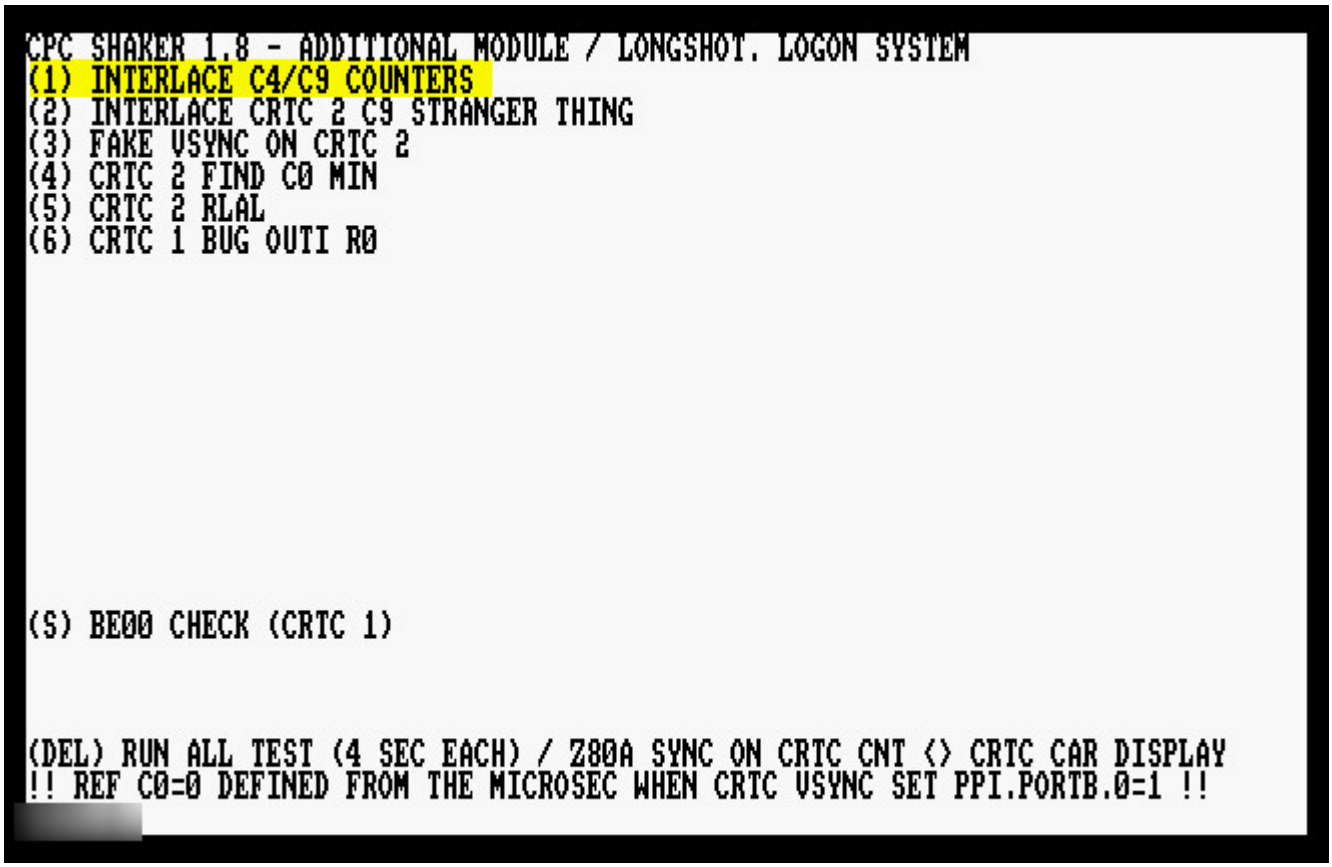
INTERLACE VM

```
CPC SHAKER 1.8 / LONGSHOT. LOGON SYSTEM
(1) UPDATE VRAM VS CRTC (14 TST)                    (0)  CRTC 2 RVMB
(2) SKEW DISP ON R0 RUPTURE (5 TST)                 (F0) BOUNGA:CRTC 2 ZERO!
(3) INTERRUPT DELAY FROM R2 (18 CALC)               (F1) INTERLACE VM (27 TST)
(4) UPDATE CRTC R0 TIMING (7 TST)
(5) R13 UPDATE IN 4 USEC SCREENS (R0=3) (5 TST)
(6) R13 UPDATE IN 2 USEC SCREENS (R0=1) (5 TST)
(7) R13 UPDATE IN 1 USEC SCREENS (R0=0) (5 TST)
(8) GATE ARRAY PIXELISATION
(9) GATE ARRAY INKERISATION (3 TST)
(E) GATE ARRAY MODERISATION
(R) HSYNC DELAY MODE UPD,UPD R2,LGTH R3 (2.1.0)(3 TST)
(T) R2 UPD DURING & AFTER HSYNC (6 TST)
(Y) R3 UPD DURING HSYNC (8 TST)
(U) R4 & R9 CHECKING (6 TST (IN PROGRESS))
(I) VSYNC CONDITIONS (16 TST)
(O) R1 STORIES (7 TST)
(P) R6 STORIES (11 TST)
(RETURN) RUNI LTD
(CAPS) ANALYZER / FORCED STAB CRTC 0 R0=0  (4 CONF)
(CTRL) R5 SCANNER / (TAB) R5 STORIES (INTERACTIVE)
(COPY) CRTC 2 OFFSET
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0vs=0 DEFINED FROM CRTC VSYNC FROM PPI.PORTB.0=1 !!
```



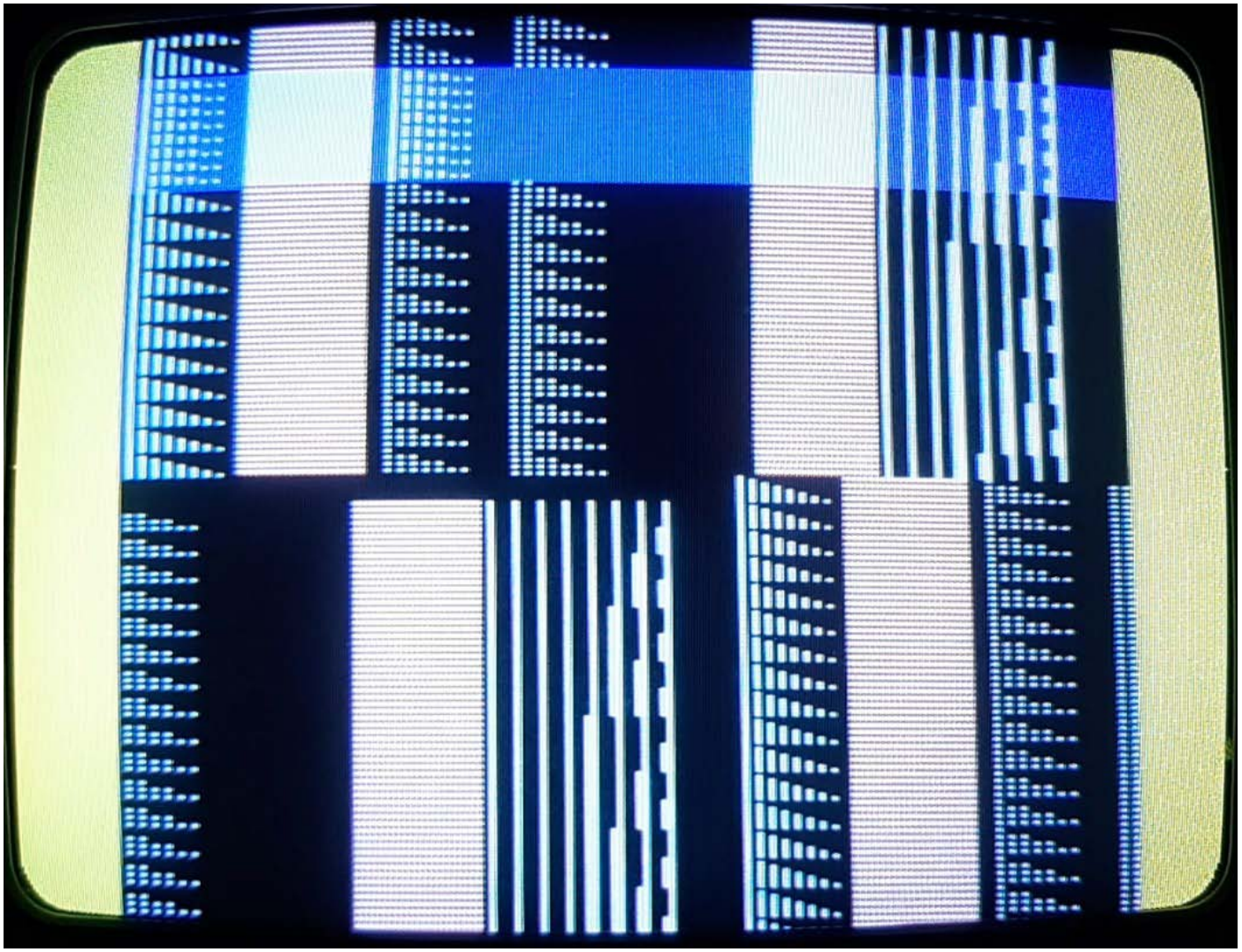

CRTC 2 INTERLACE VIDEO MODE
R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#4E20 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#4E20 usec (R9=7)
R8 UPDATE DELAY + 0 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#4E20 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#4E20 usec (R9=7)
R8 UPDATE DELAY + 1 FRAME DELAY
R8=3 ON C9=0, C0=#3D : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON C9=0, C0=#3E : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON C9=0, C0=#3F : FRAME SIZE=#4E60 usec (R9=7)
R8=3 ON C9=1, C0=#00 : FRAME SIZE=#4E40 usec (R9=7)
R8=3 ON C9=1, C0=#01 : FRAME SIZE=#4E40 usec (R9=7)
DELAY FOR EVEN+ODD FRAME (E/O R6=50/50,7F/50,50/7F,7F/7F)
R8=3 ON LINE 0 : FRAME SIZE=#9C60 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9C40 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9C80 usec (R9=7)(R7=0)
R8=3 ON LINE 0 : FRAME SIZE=#9C80 usec (R9=7)(R7=0)

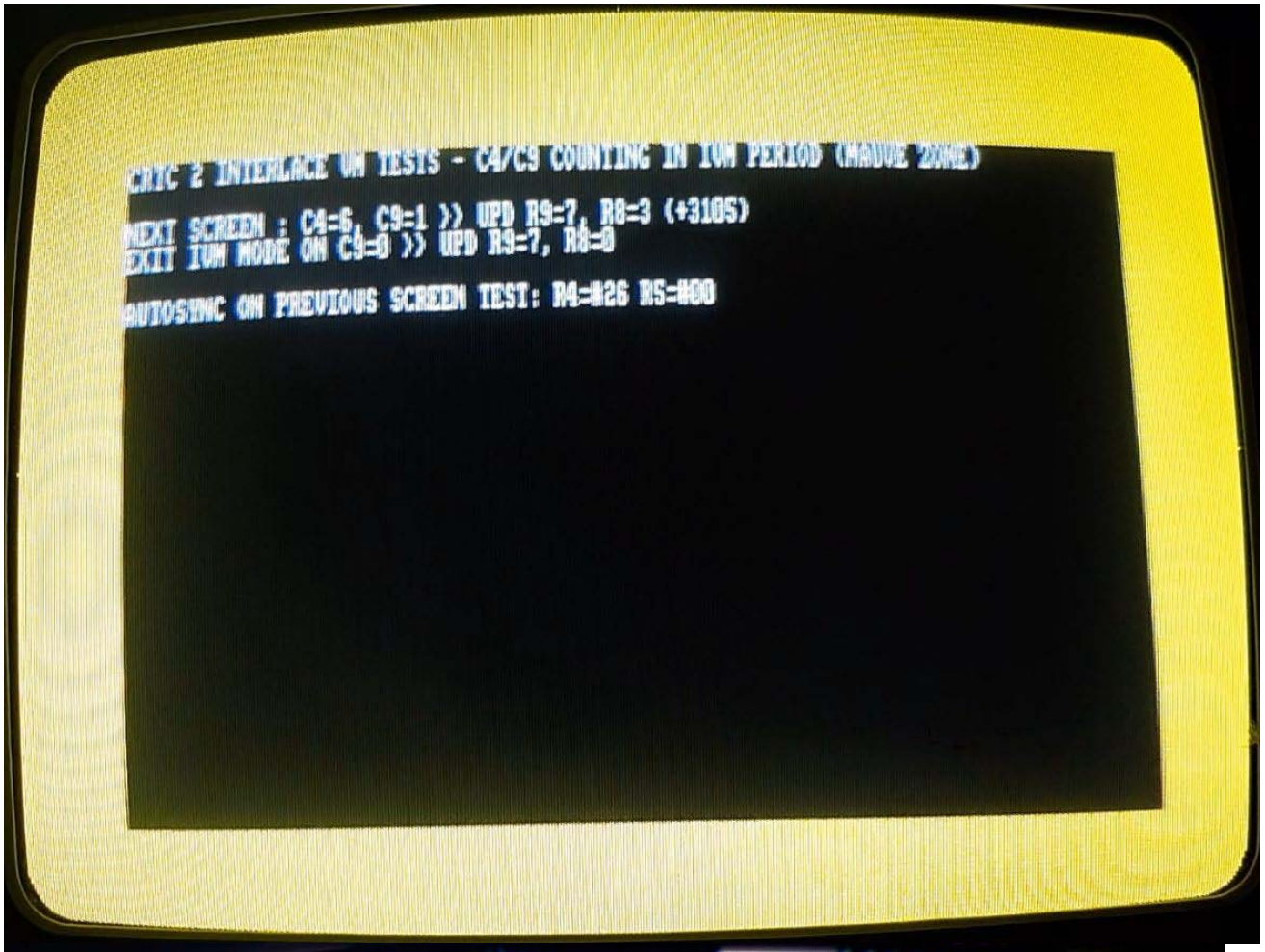
INTERLACE C4/C9 COUNTERS



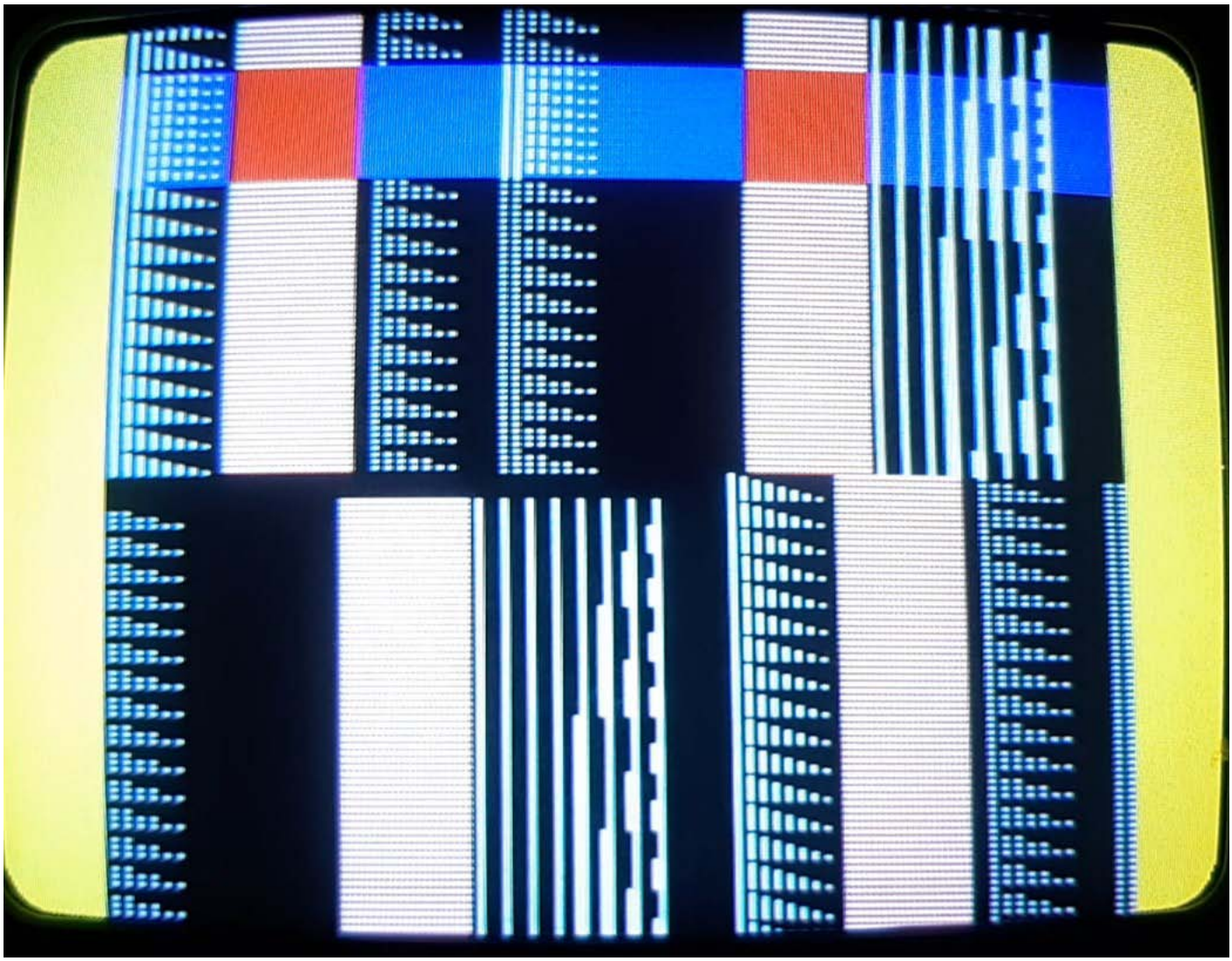

CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MOUVE ZONE)
NEXT SCREEN : C4=6, C9=0)) UPD R9=7, R8=3 (+3105)
EXIT IVH MODE ON C9=0)) UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=0xx R5=0xx

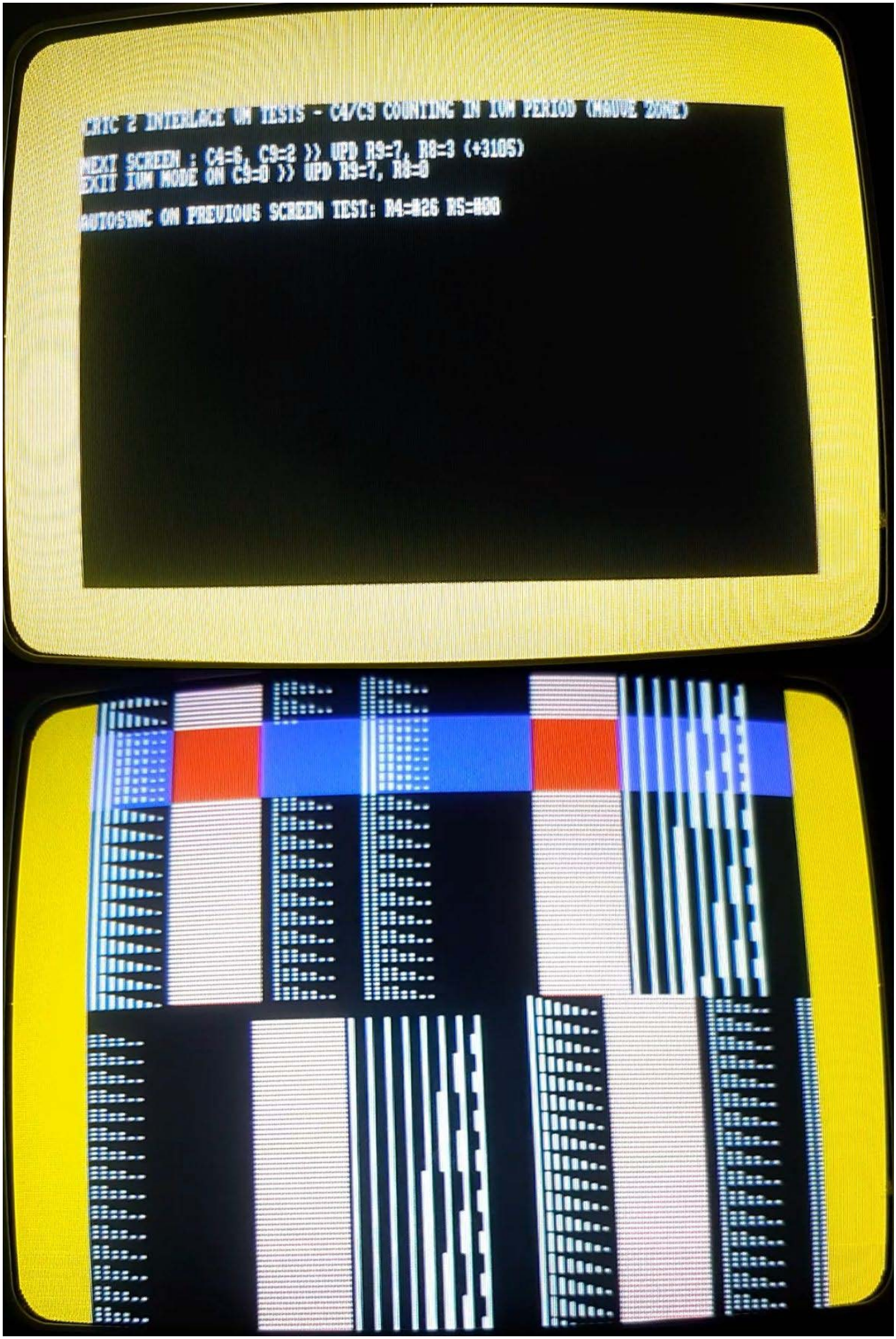
Or this

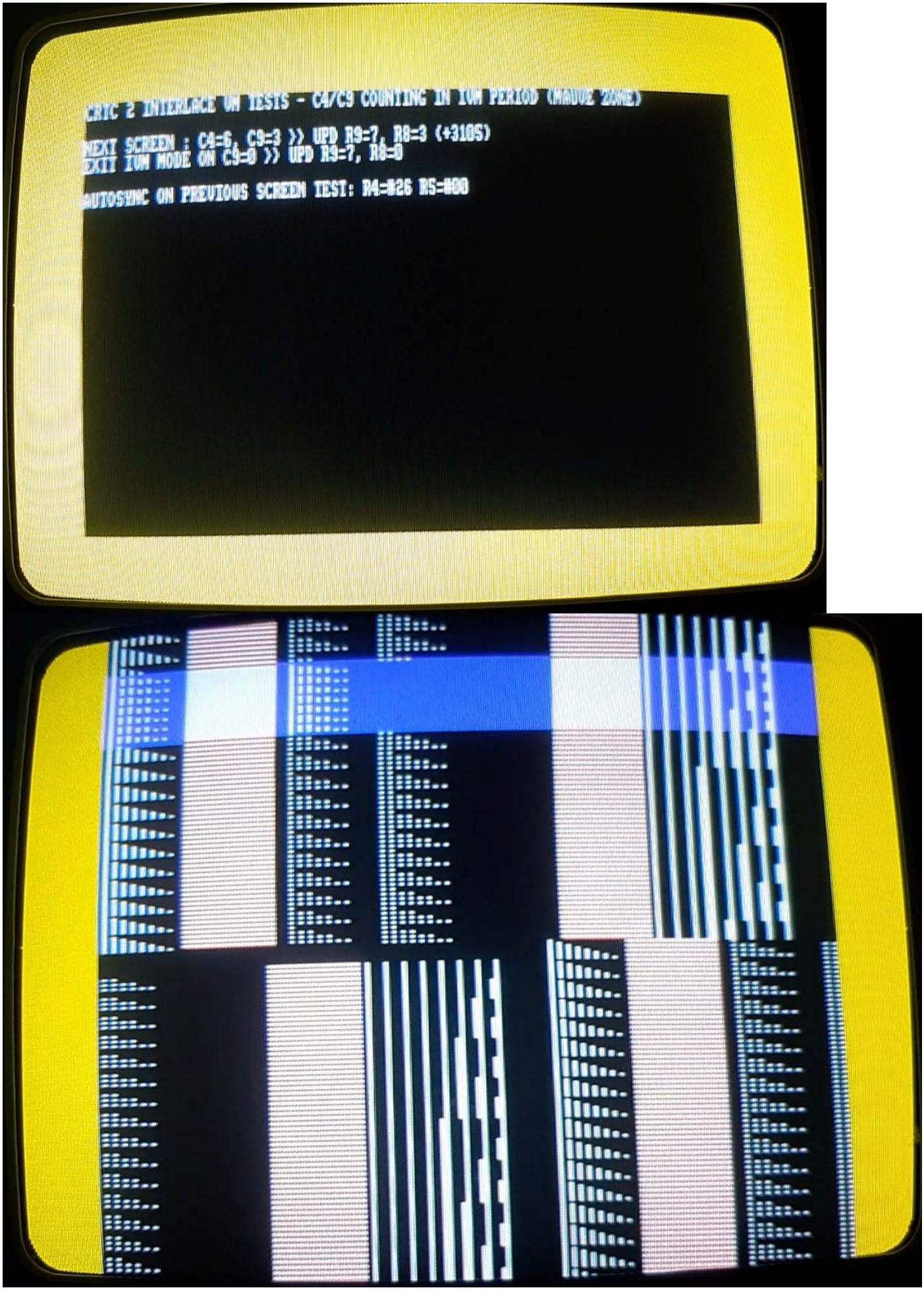



CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=1 >> UPD R9=7, R8=3 (+3105)
EXIT IVW MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00

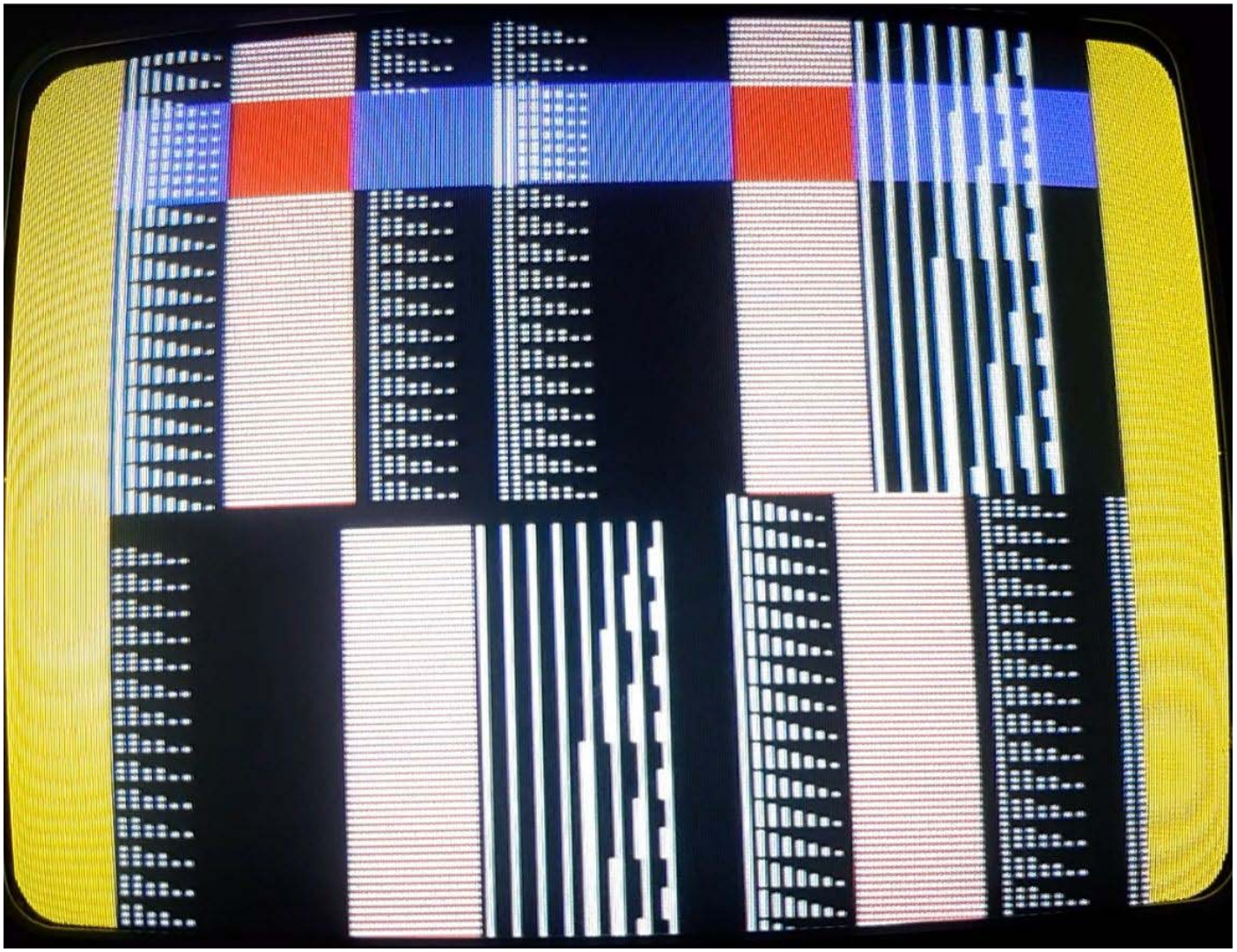
Or this

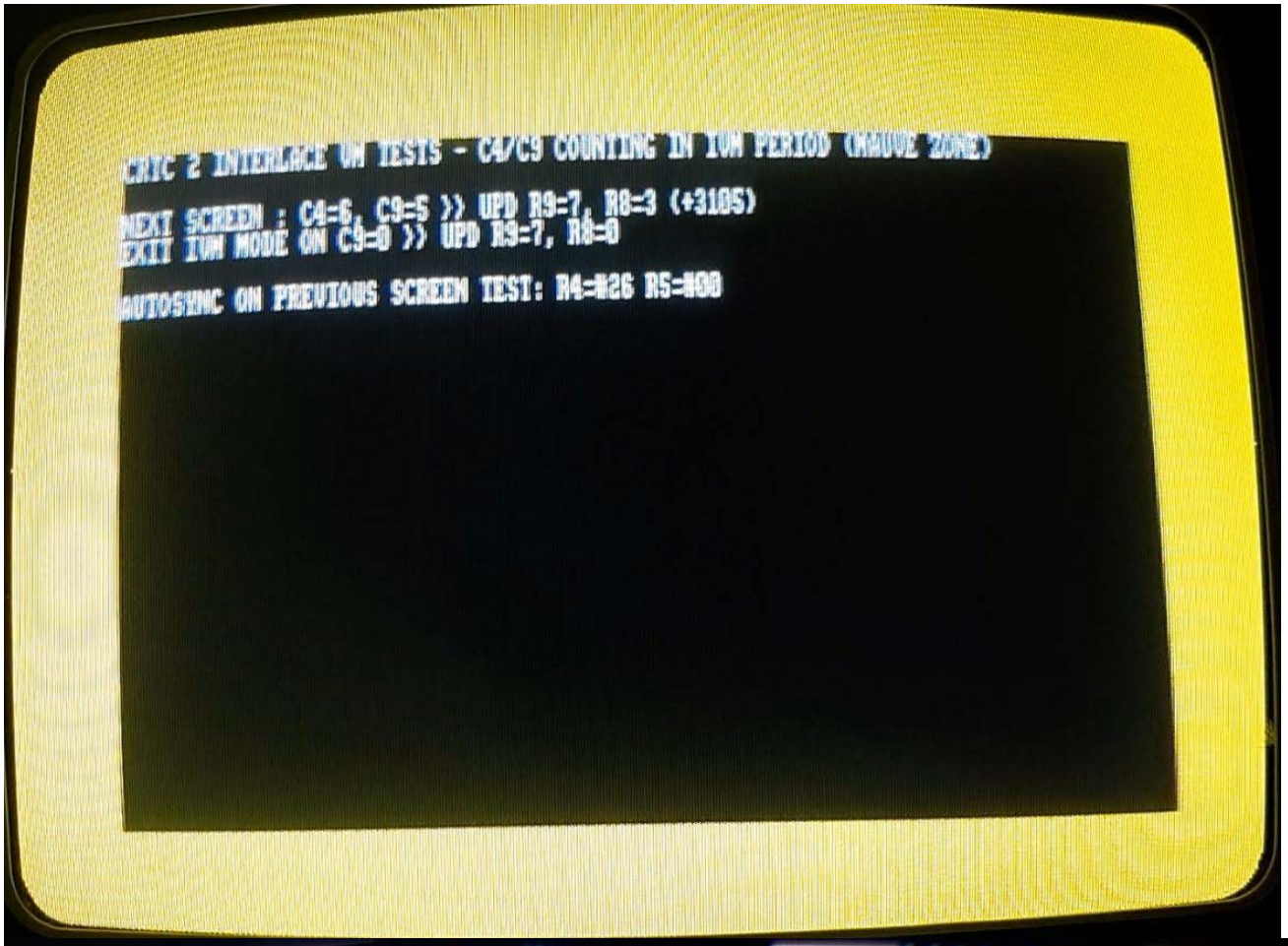


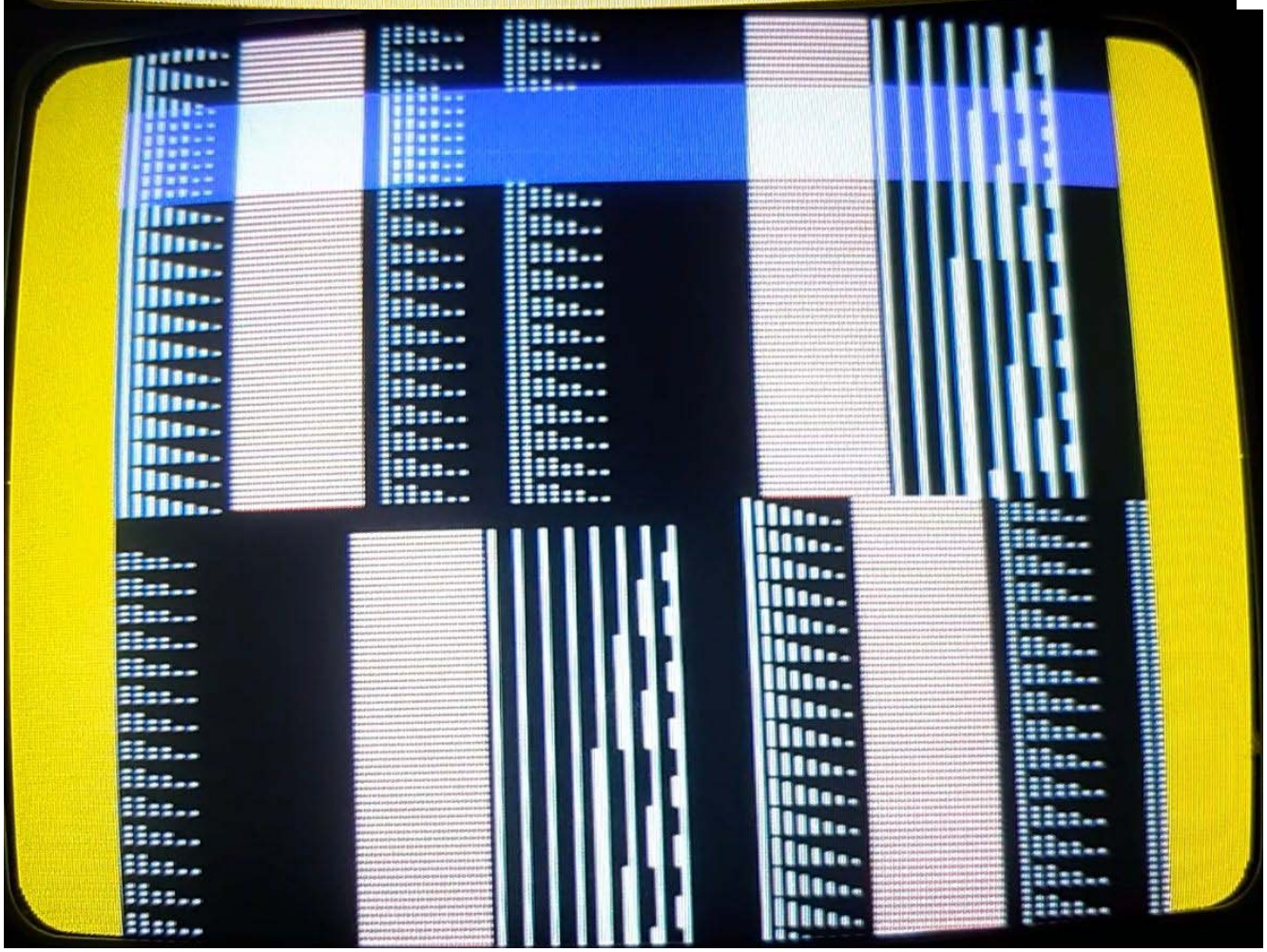

CRTC 2 INTERLACE ON TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=2)) UPD R9=7, R8=3 (+3105)
EXIT IVW MODE ON C9=0)) UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00


CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MODUE ZONE)
NEXT SCREEN : C4=6, C9=3 >> UPD R9=7, R8=3 (+310S)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00

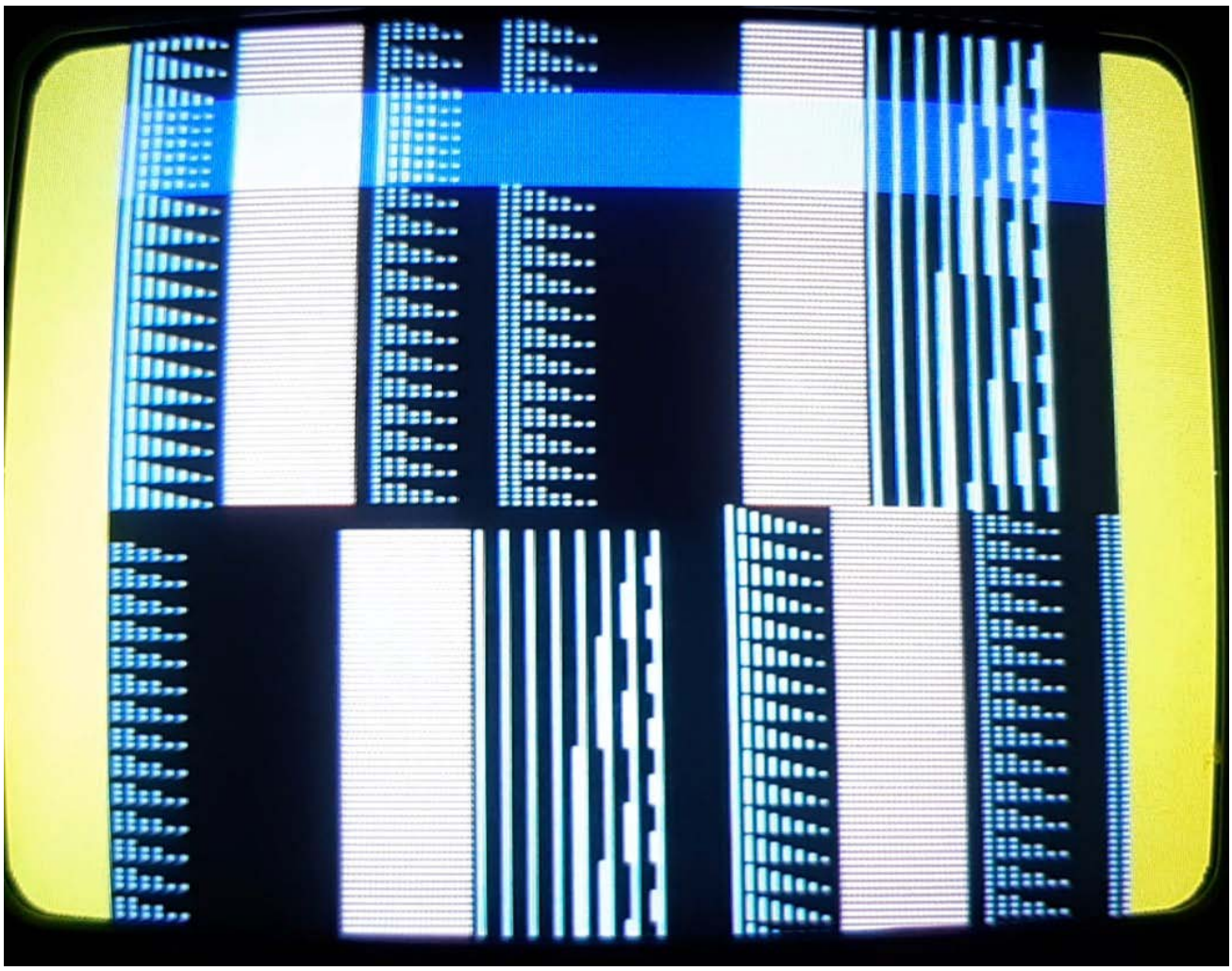

CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MODUE 2&ME)
NEXT SCREEN : C4=6, C9=4 >> UPD R9=7, R8=3 (+3105)
EXIT IVH MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00



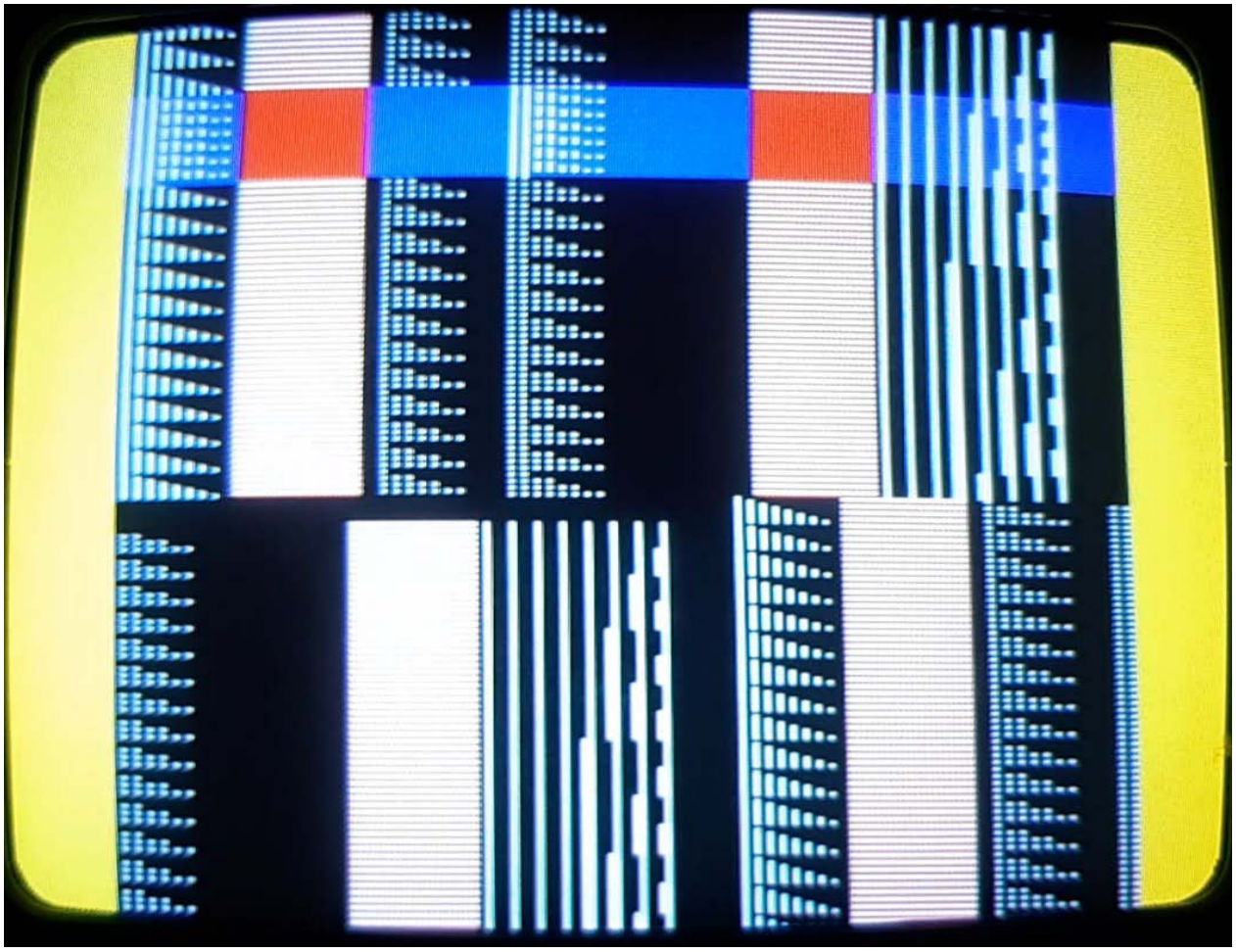

CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (ABOVE ZONE)
NEXT SCREEN : C4=6, C9=5)) UPD R9=7, R8=3 (+3105)
EXIT IVH MODE ON C9=0)) UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00



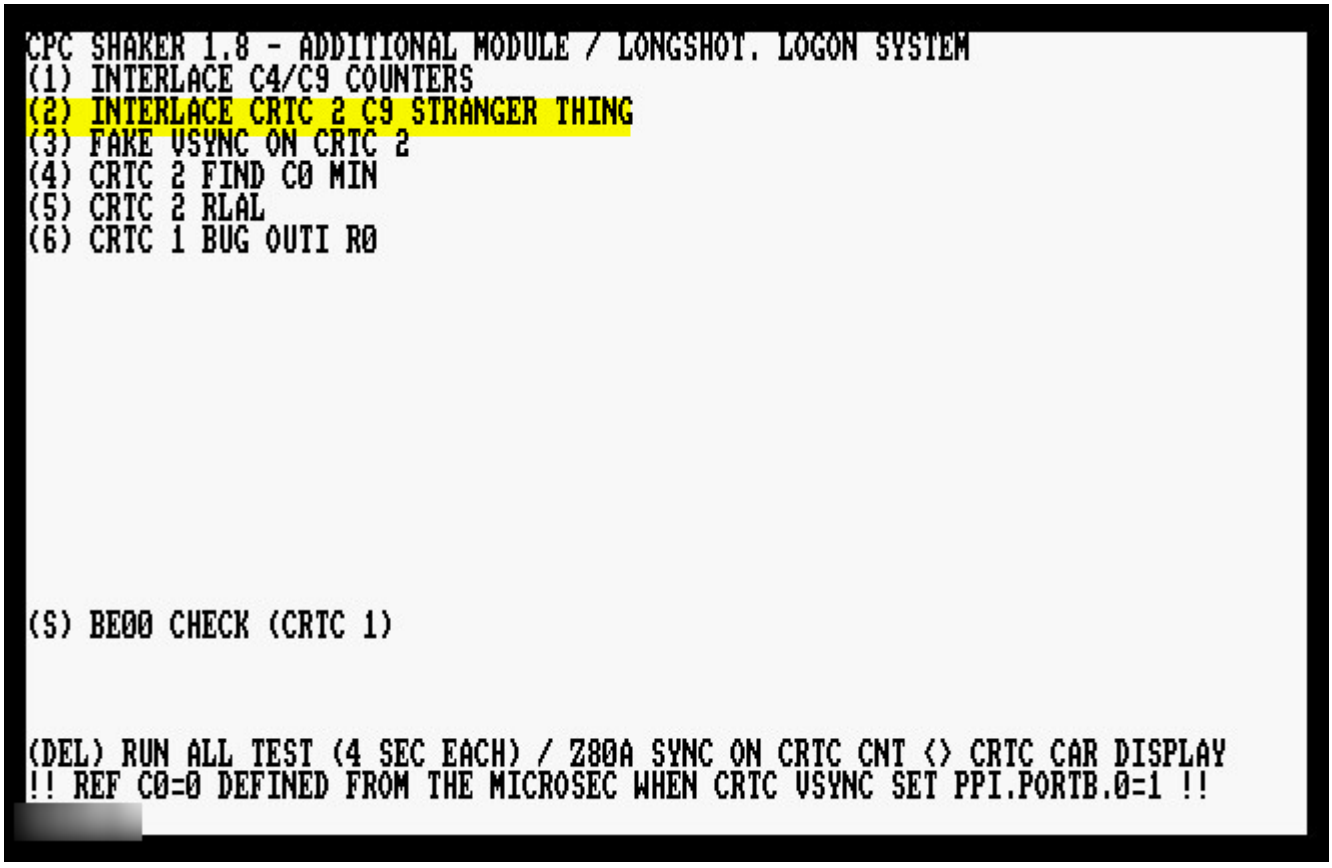

CRTC 2 INTERLACE VH TESTS - C4/C9 COUNTING IN IVH PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=6 >> UPD R9=7, R8=3 (+3105)
EXIT IVH MODE ON C9=8 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00

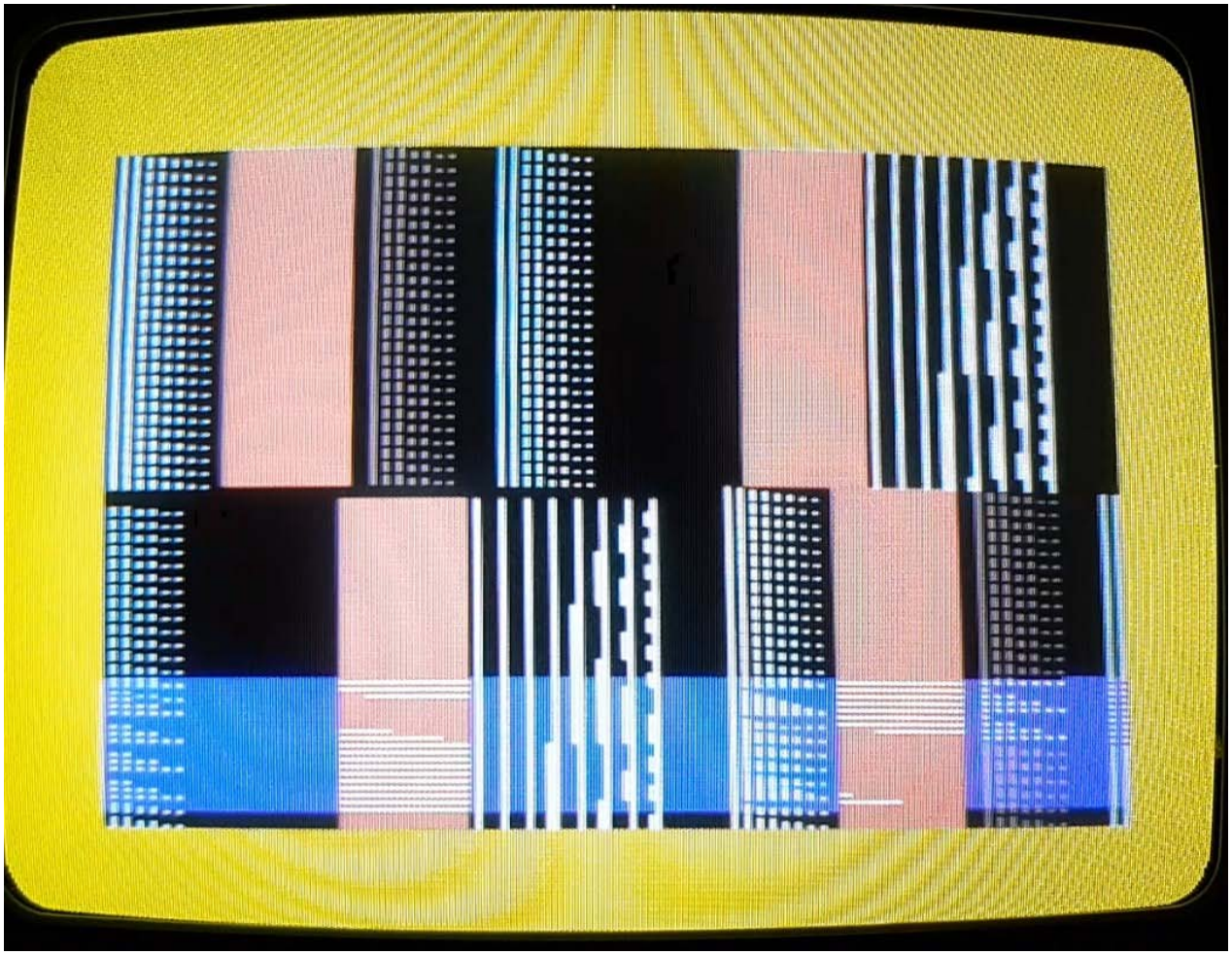



CRTC 2 INTERLACE VW TESTS - C4/C9 COUNTING IN IVW PERIOD (MAUVE ZONE)
NEXT SCREEN : C4=6, C9=7 >> UPD R9=7, R8=3 (+3105)
EXIT IVW MODE ON C9=0 >> UPD R9=7, R8=0
AUTOSYNC ON PREVIOUS SCREEN TEST: R4=#26 R5=#00



INTERLACE CRTC 2 C9 STRANGER THING





FAKE VSYNC ON CRTC 2

```
CPC SHAKER 1.8 - ADDITIONAL MODULE / LONGSHOT. LOGON SYSTEM
(1) INTERLACE C4/C9 COUNTERS
(2) INTERLACE CRTC 2 C9 STRANGER THING
(3) FAKE VSYNC ON CRTC 2
(4) CRTC 2 FIND C0 MIN
(5) CRTC 2 RLAL
(6) CRTC 1 BUG OUTI R0







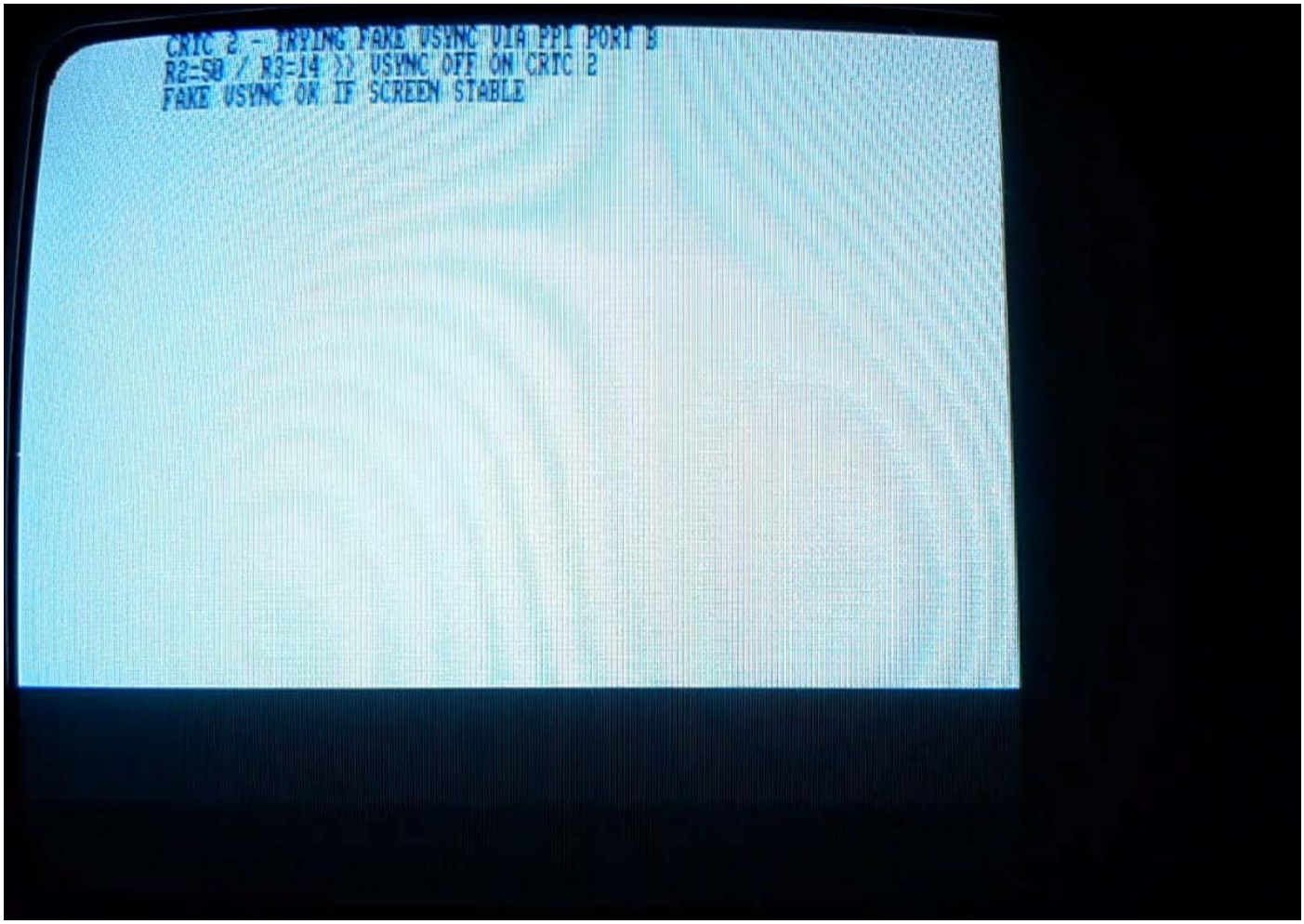


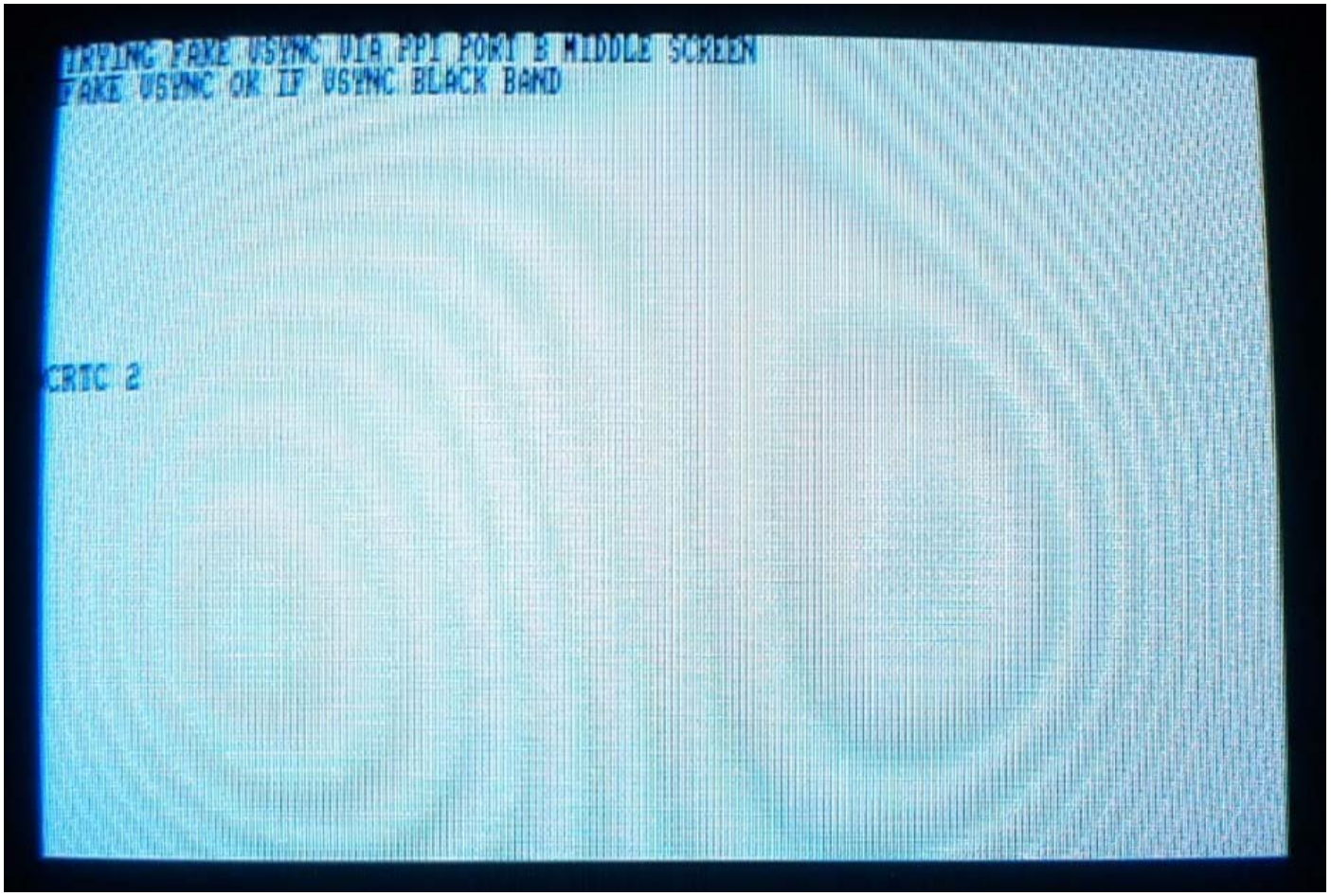
(S) BE00 CHECK (CRTC 1)



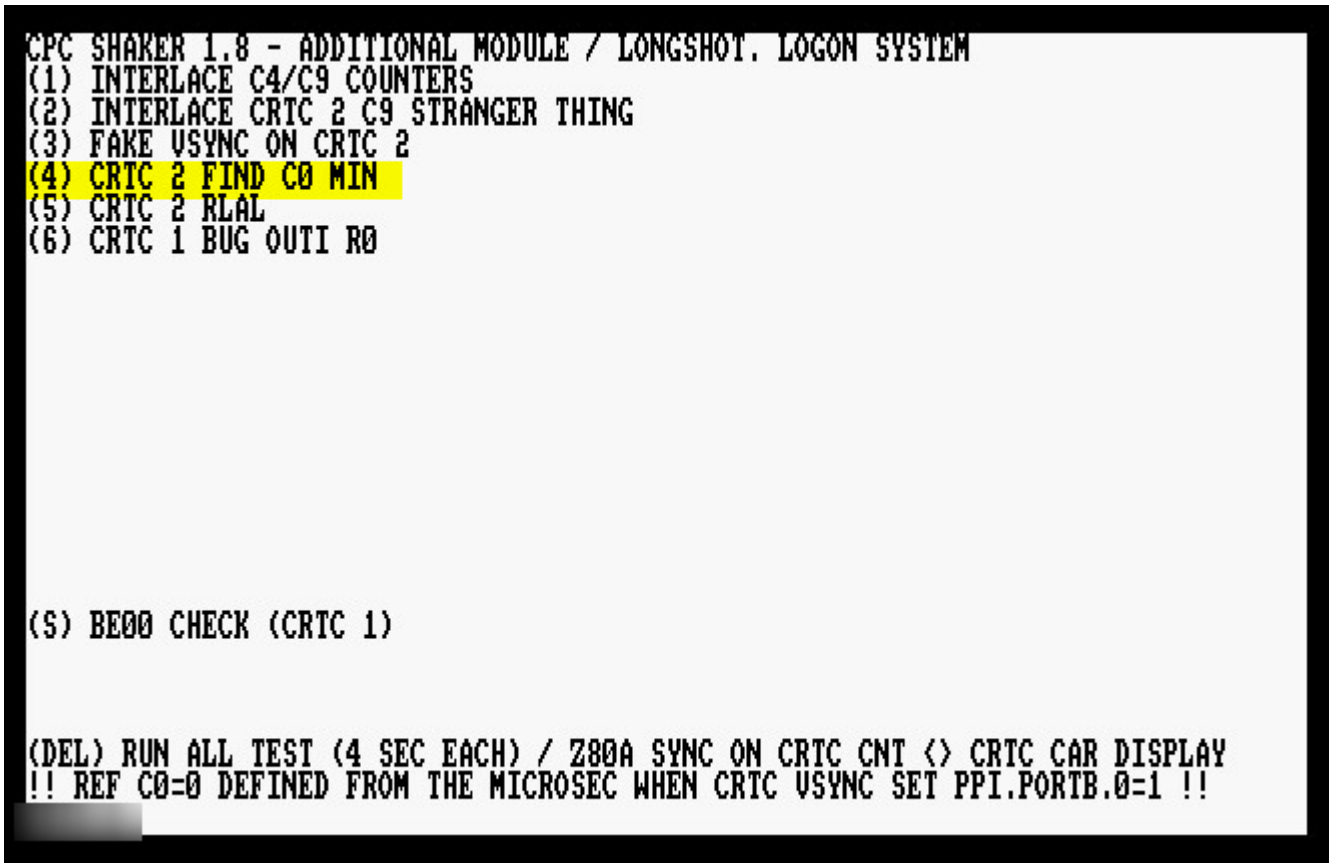
(DEL) RUN ALL TEST (4 SEC EACH) / Z80A SYNC ON CRTC CNT <> CRTC CAR DISPLAY
!! REF C0=0 DEFINED FROM THE MICROSEC WHEN CRTC VSYNC SET PPI.PORTB.0=1 !!
```

Not Stable

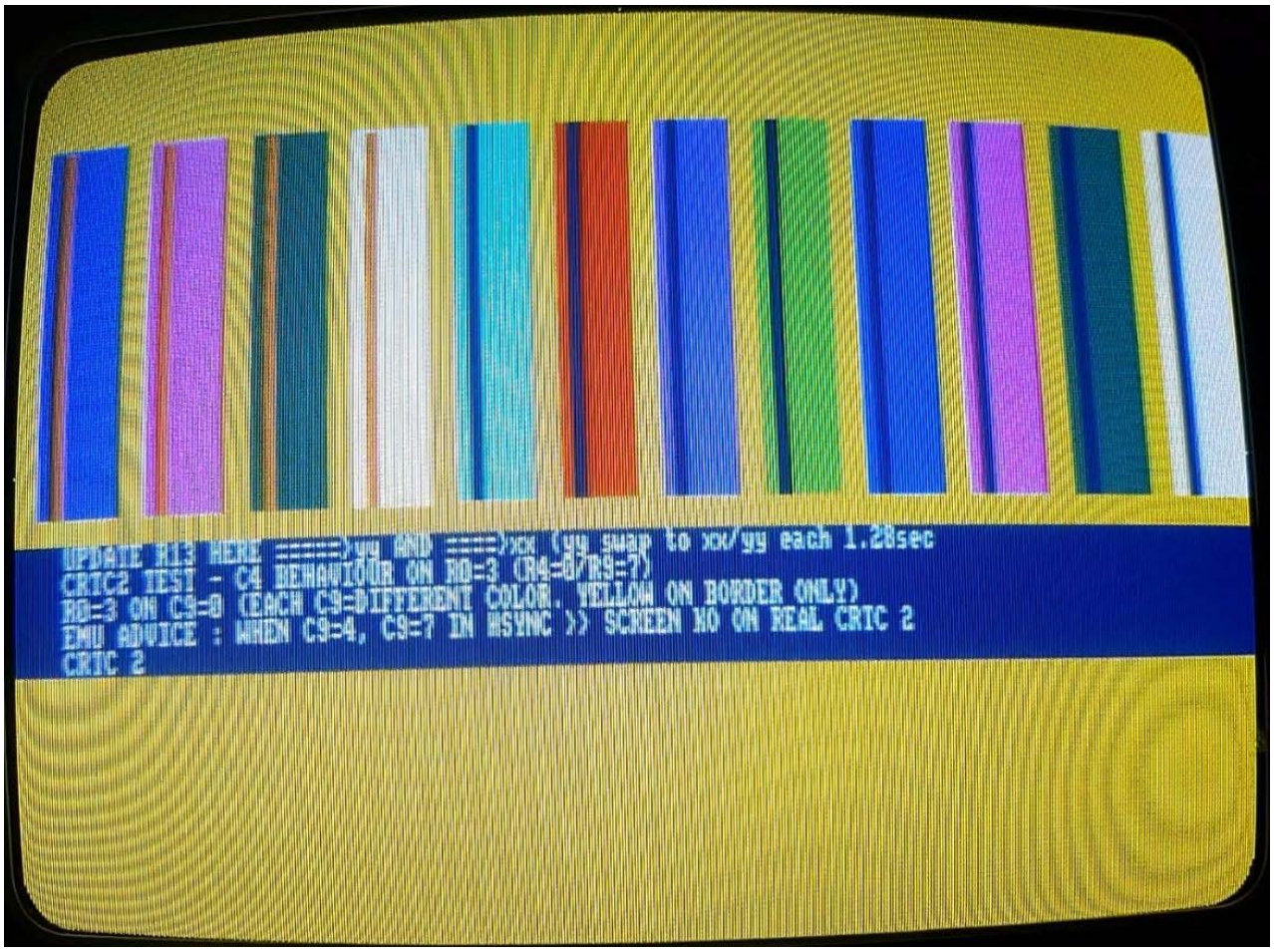



MAPPING FAKE VSYNC VIA PPI PORT B MIDDLE SCREEN
FAKE VSYNC OK IF VSYNC BLACK BAND
CRTC 2

CRTC 2 FIND C0 MIN



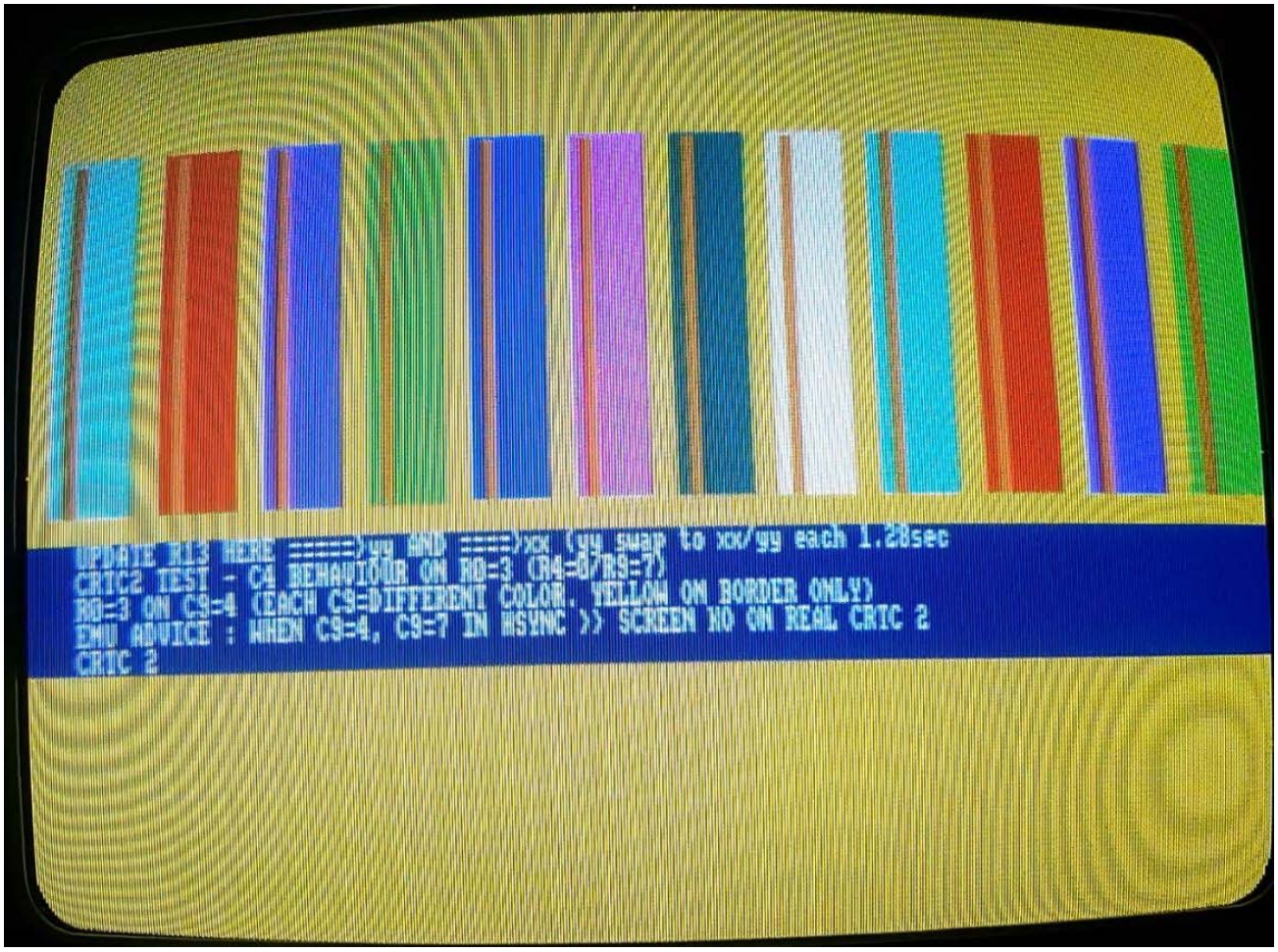

UPDATE R13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=0 (EACH C9=DIFFERENT COLOR, YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN KO ON REAL CRTC 2
CRTC 2

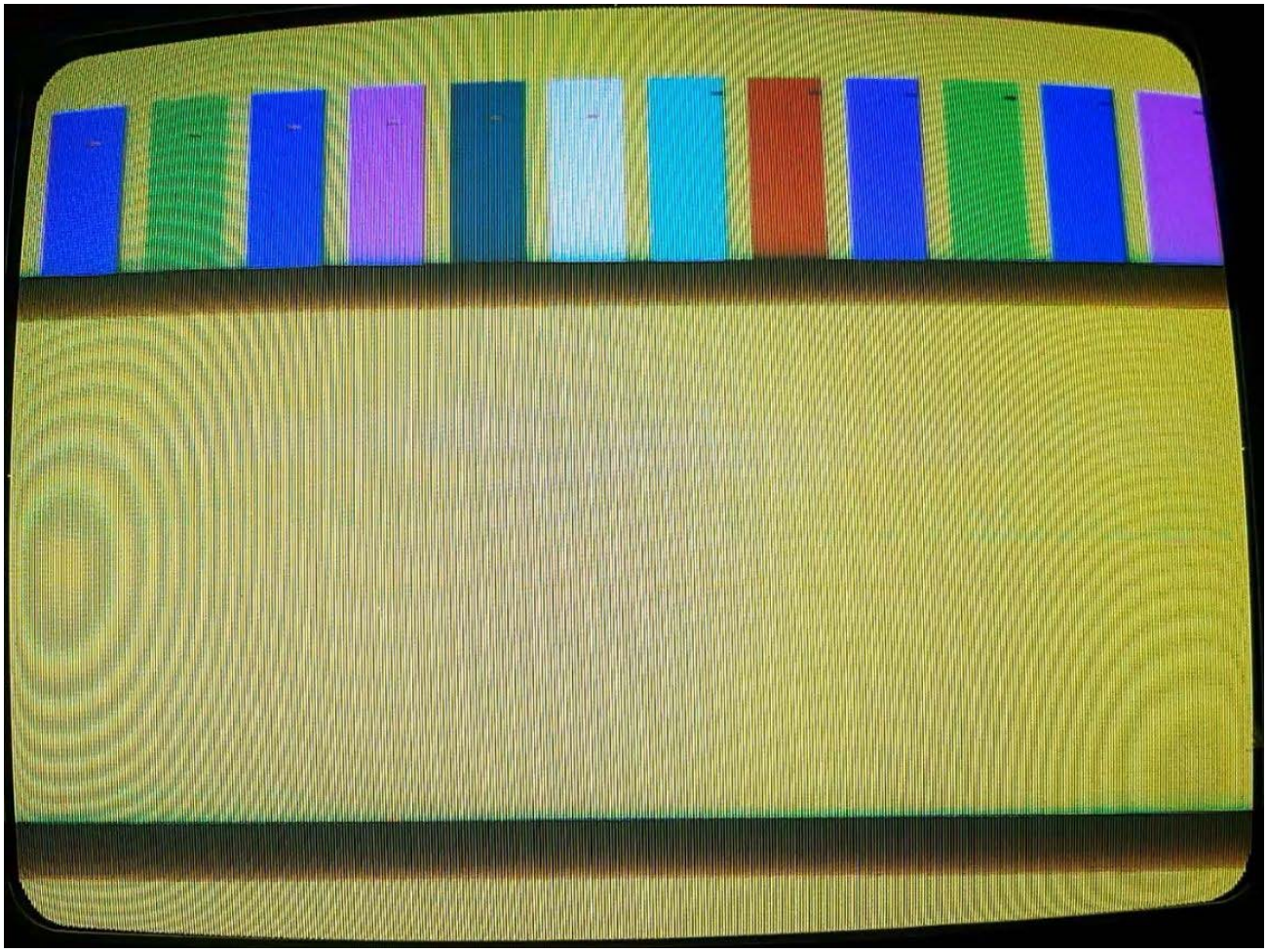

UPDATE R13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=0 (EACH C9=DIFFERENT COLOR, YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN KO ON REAL CRTC 2
CRTC 2


UPDATE R13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=1 (EACH C9=DIFFERENT COLOR. YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN KO ON REAL CRTC 2
CRTC 2

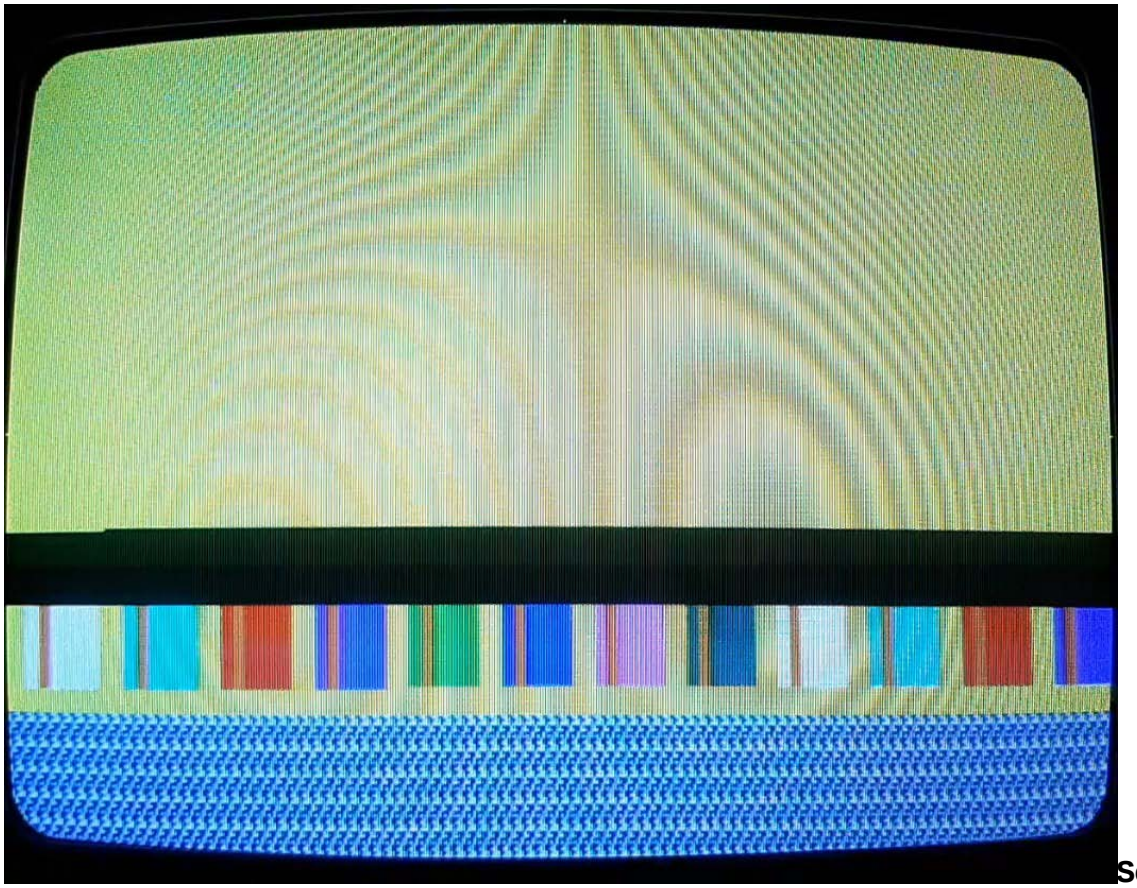

UPDATE R13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=2 (EACH C9=DIFFERENT COLOR. YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN KO ON REAL CRTC 2
CRTC 2


UPDATE $13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=3 (EACH C9=DIFFERENT COLOR, YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN NO ON REAL CRTC 2
CRTC 2


UPDATE $13 HERE =====>yy AND ====>xx (yy swap to xx/yy each 1.28sec
CRTC2 TEST - C4 BEHAVIOUR ON R0=3 (R4=0/R9=7)
R0=3 ON C9=4 (EACH C9=DIFFERENT COLOR, YELLOW ON BORDER ONLY)
EMU ADVICE : WHEN C9=4, C9=7 IN HSYNC >> SCREEN NO ON REAL CRTC 2
CRTC 2

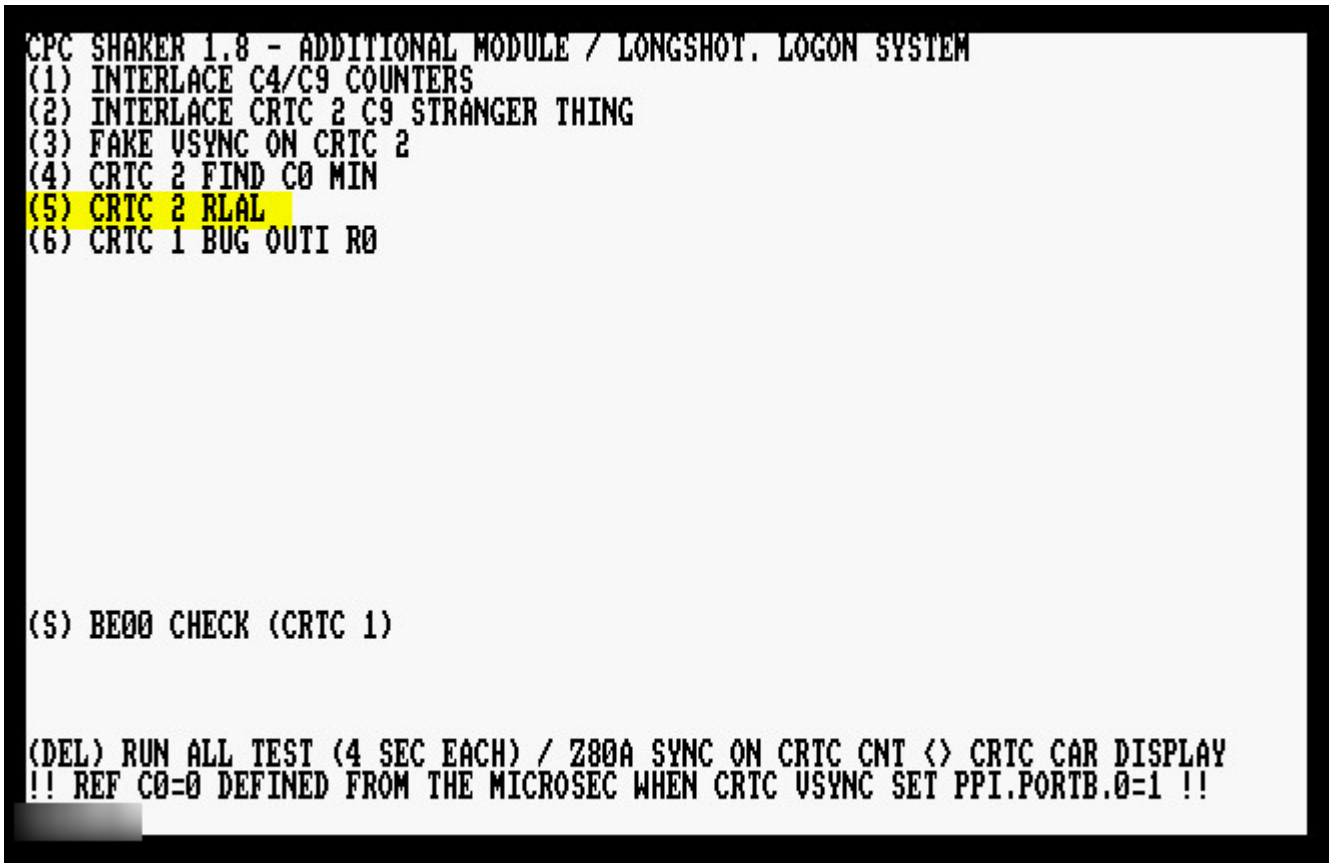


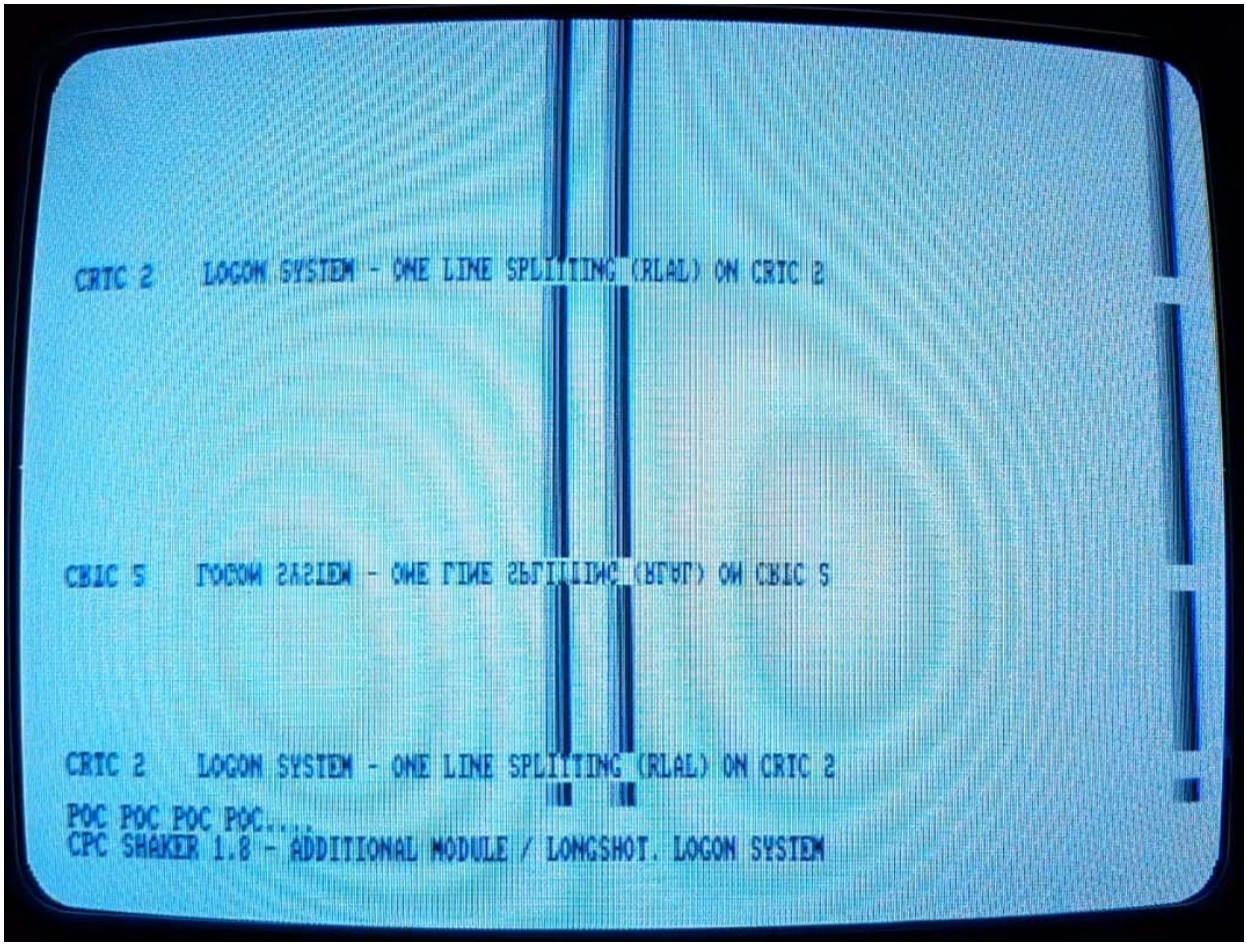
Screen KO (compare to CRTC 1 for stable screen)

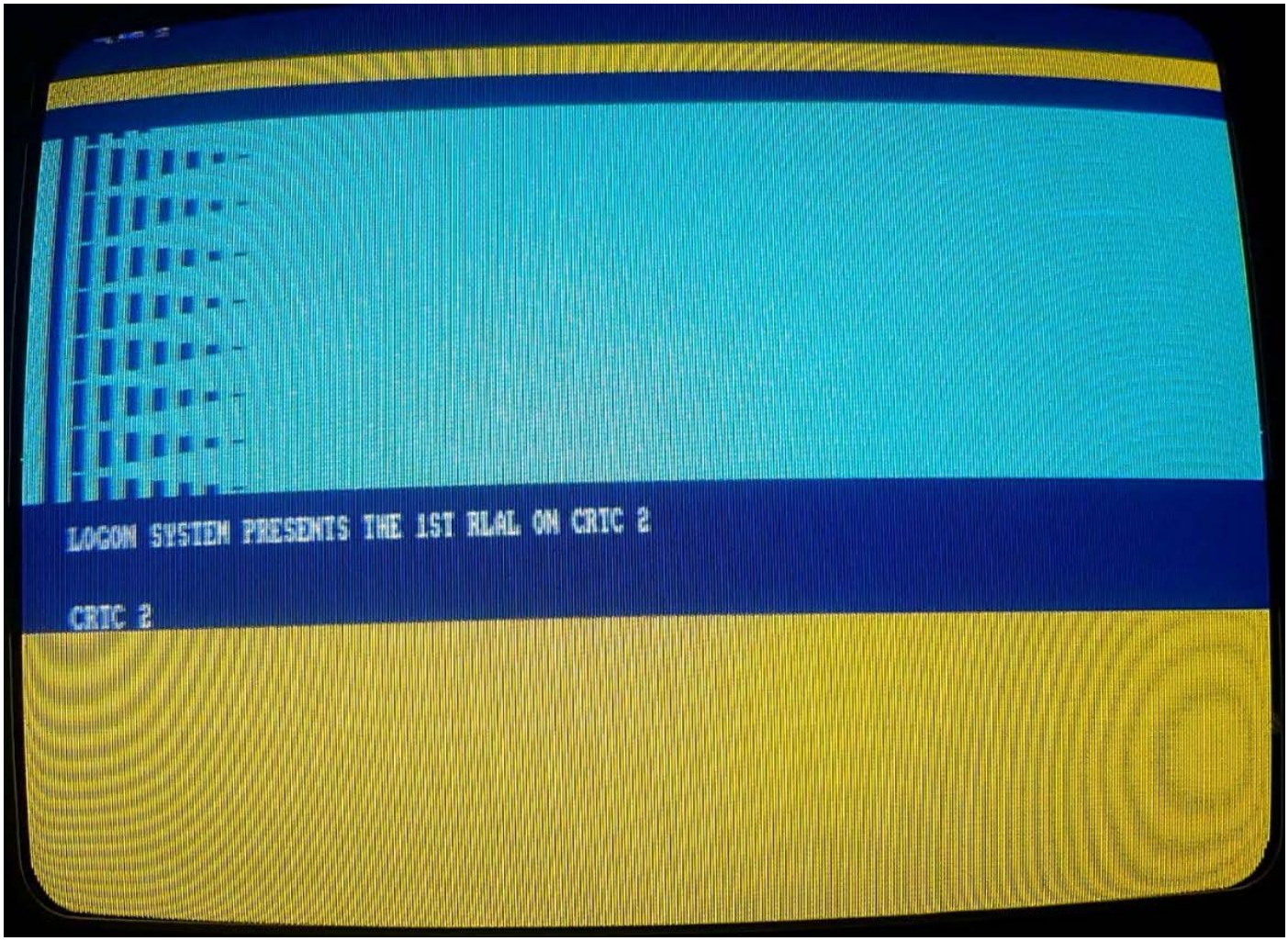


Screen KO (compare to CRTC 1 for stable screen)

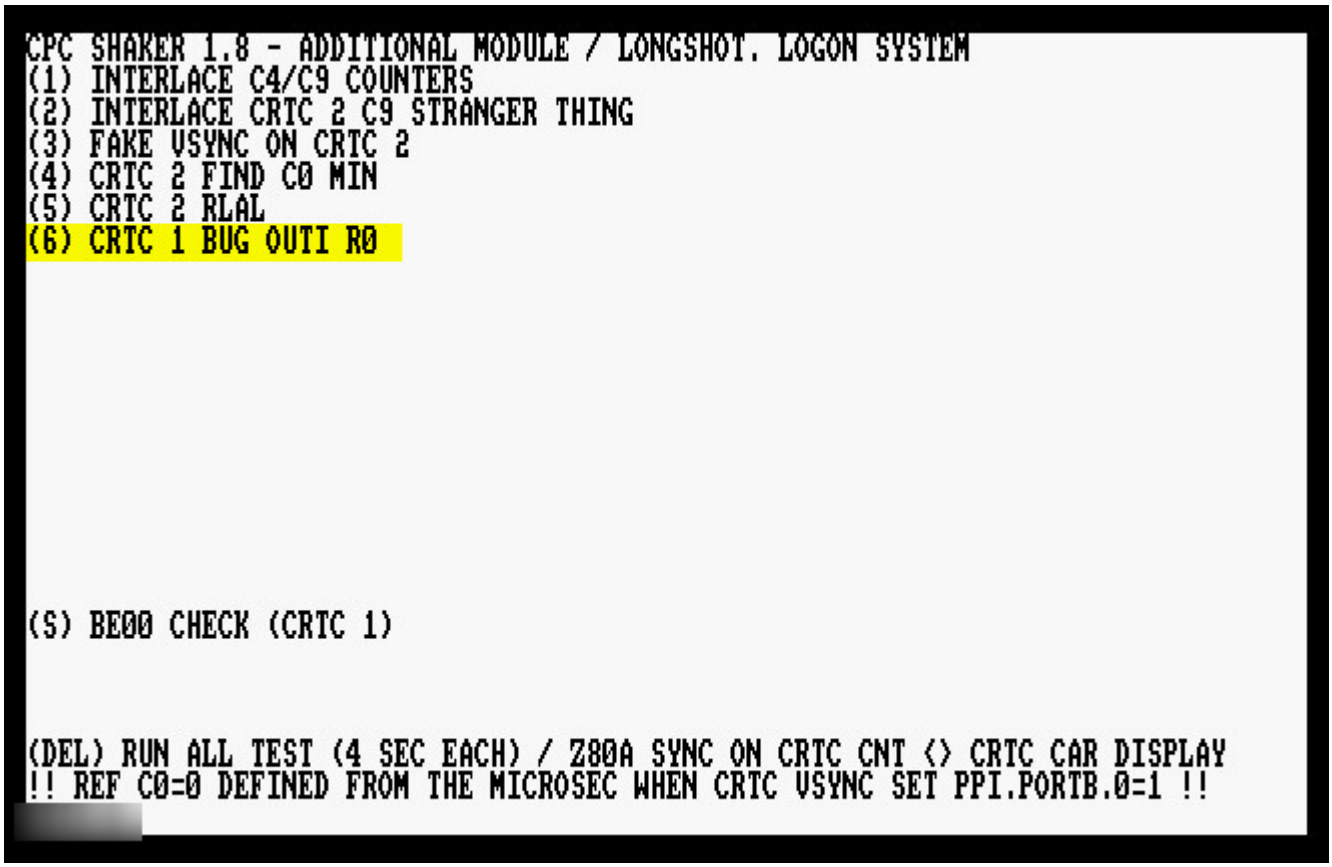
CRTC 2 - 1 LINE RUPTURE





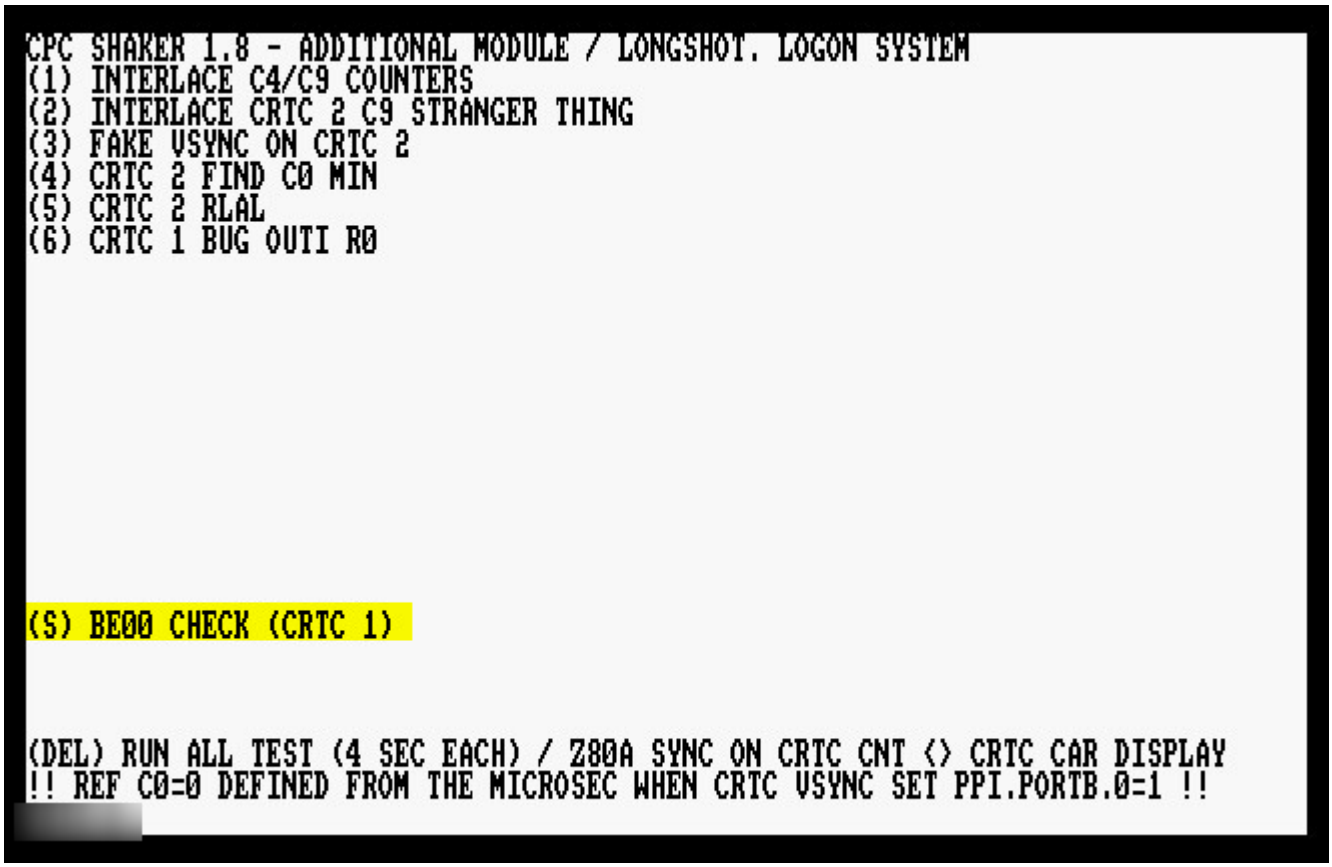

LOGON SYSTEM PRESENTS THE 1ST REAL ON CRIC 2
CRIC 2

CRTC 1 – BUG OUTI R0



Only for CRTC 1

CRTC 1- BE00 CHECK



Only for CRTC 1